

XD1602A0

(Dot-Matrix Liquid Crystal Display One-Chip Controller/Driver
Supporting Korean/Japanese/Russian/Latin Font Display)

NSYTECH

Description

The XD1602A0 is a dot-matrix liquid crystal display controller (LCD) and driver LSI that displays Korean characters consisting of hiragana and katakana according to the Korean Industrial Standard KSC 5601. The XD1602A0 incorporates the following five functions on a single chip: (i) display control function for the dot matrix LCD, (ii) a display RAM to store character codes, (iii) ROM fonts to support Korean, (iv) liquid crystal driver, and (v) a booster to drive the LCD. A two 16-character (XD1602A0) Korean display can easily be achieved by receiving character codes (2 bytes/character) from the MPU.

The font ROM includes 2,350 Korean characters from the KSC5601 Set, and 128 half-size alphanumeric characters and symbols. Full-size fonts such as Korean/Japanese/English/Russian/Latin and half-size of fonts such as alphanumeric characters can be displayed together.

In addition, display control equivalent to full bit mapping can be performed through horizontal and vertical dot-by-dot smooth scroll functions for each display line.

Features

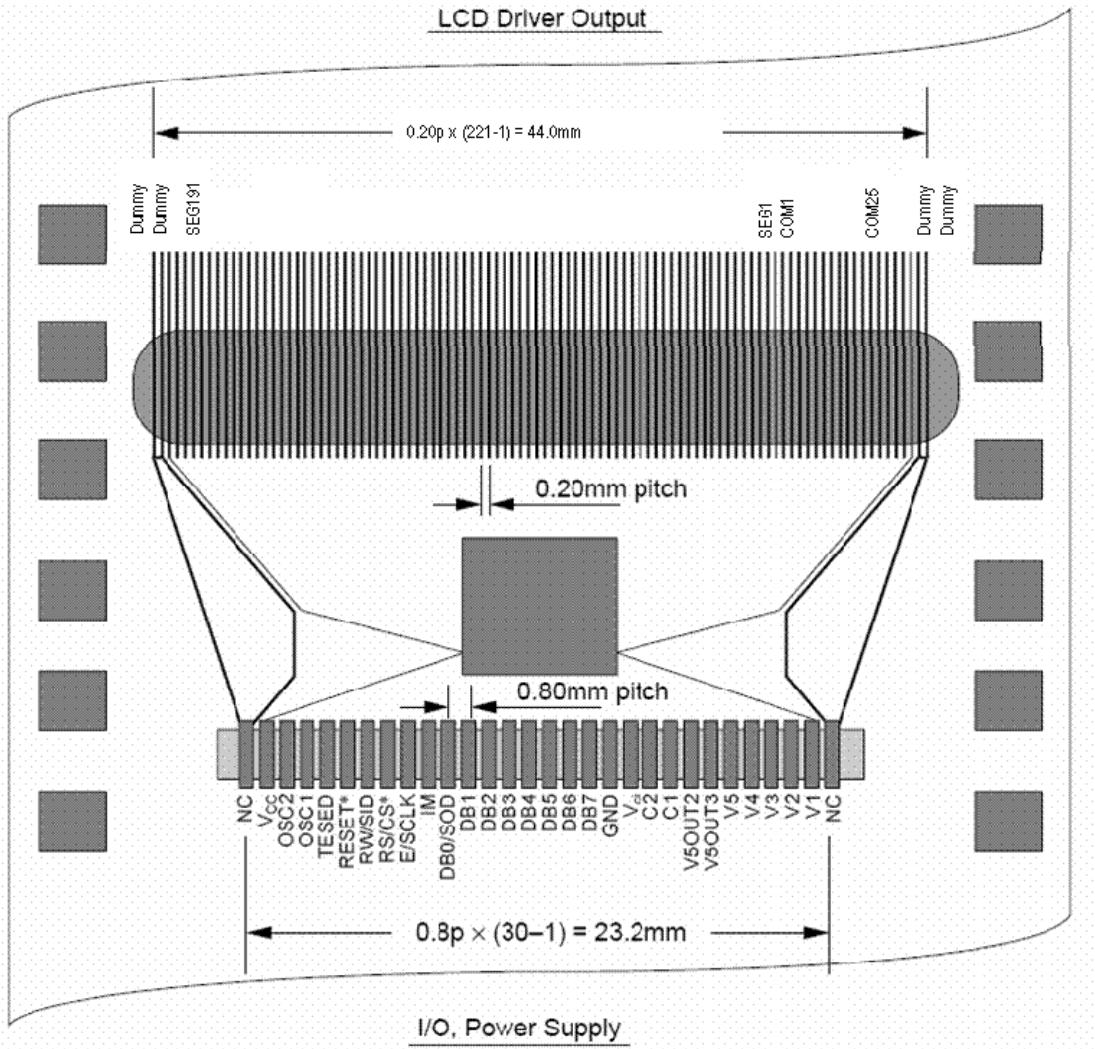
- Dot-matrix liquid crystal display controller/driver supporting the display of Korean according to KSC5601 Set
- Large character generator ROM: 510 kbits
 - Korean according to KSC5601 Set (11 × 12 dots): 2,350-character font
 - Includes KOREAN Alphabet (11 × 12 dots): 96-character font
 - Includes Full-size Hiragana and katakana Full size character font(11 × 12 dots)
 - Includes Full-size Russian Full size character font(11 × 12 dots)
 - Includes Full-size Alphabet font of Gothic type / Alphabet font of Roman type(11 × 12 dots)
 - Includes Full-size Latin font of four type(11 × 12 dots)
 - Half-size alphanumeric characters and symbols (5 × 12 dots): 128-character font
- Display of 11 × 12 dots for full-size fonts consisting of Korean, 5 × 12 dots for half-size fonts of alphanumeric characters and symbols in the same display
- 2-line 16-character full-size font display with a single chip (XD1602A0)

- Various display control functions: horizontal smooth scroll (in dot units), vertical smooth scroll, white black inversion/blinking/white black inversion blinking character display, cursor display, display on/off
- Display data RAM: 40×2 bytes (stores codes to support 40 characters in a full-size font)
- Character generator RAM: 8×26 bytes (displays 8 characters of a 12×13 dot user font)
- 16-byte 191-segment RAM
- 8-bit bus interface
- Built-in double liquid-crystal voltage booster circuit and built-in oscillator (operating frequency can be adjusted through external resistors)
- Operating power supply voltage: 4.5V to 5.5V; liquid crystal display voltage: 3.0V to 13.0V
- XD1602A0: bare-chip

MANUAL REVISION RECORD

- 2006-01-10 : First Release, Version 0.1
- 2007-01-10 : Second Release, Version 1.0
- 2008-03-17 : Third Release, Version 1.1
- 2008-06-19 : Fourth Release, Version 1.1.1

TCP Dimensions (XD1602A0)



The Location of Bonding Pads (XD1602A0)

Project name : XD1602

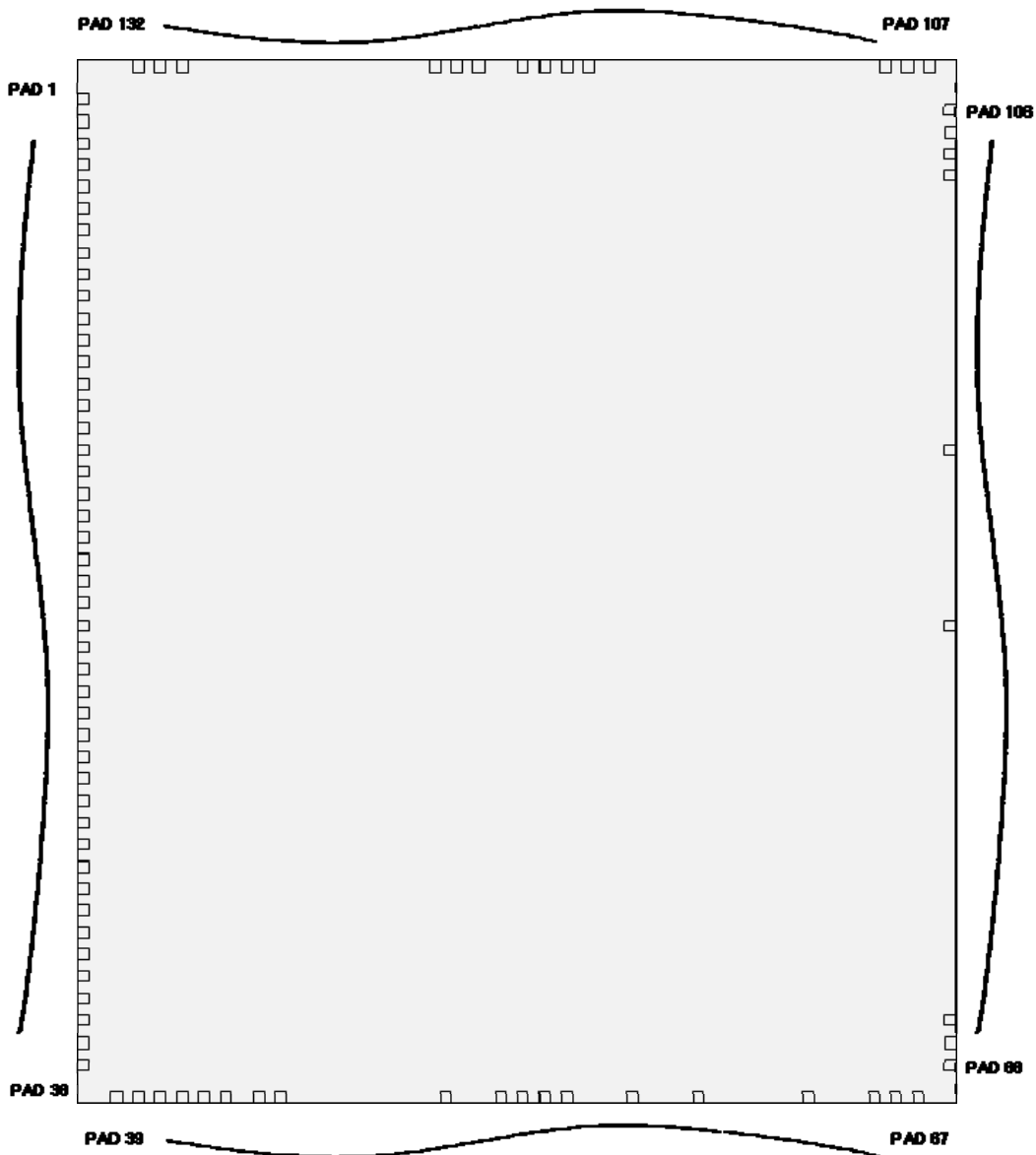
Package Type : COB

Chip Size : 3637.9um x 4852.625um

Logo : XD1602A0 (3428, 57) , Location : The right side of Bottom

PAD Size : 75um X 75um

Designer : Dean



Left (From Top to Bottom)				
pad number	Name	X	Y	Comment
1	seg[34]	42.500	4369.625	
2	seg[35]	42.500	4269.625	
3	seg[36]	42.500	4169.625	
4	seg[37]	42.500	4069.625	
5	seg[38]	42.500	3969.625	
6	seg[39]	42.500	3869.625	
7	seg[40]	42.500	3769.625	
8	seg[41]	42.500	3669.625	
9	seg[42]	42.500	3569.625	
10	seg[43]	42.500	3469.625	
11	seg[44]	42.500	3369.625	
12	seg[45]	42.500	3269.625	
13	seg[46]	42.500	3169.625	
14	seg[47]	42.500	3069.625	
15	seg[48]	42.500	2969.625	
16	seg[49]	42.500	2869.625	
17	seg[50]	42.500	2769.625	
18	seg[51]	42.500	2669.625	
19	seg[52]	42.500	2569.625	
20	seg[53]	42.500	2469.625	
21	seg[54]	42.500	2369.625	
22	seg[55]	42.500	2269.625	
23	seg[56]	42.500	2169.625	
24	seg[57]	42.500	2069.625	
25	seg[58]	42.500	1969.625	
26	seg[59]	42.500	1869.625	
27	seg[60]	42.500	1769.625	
28	seg[61]	42.500	1669.625	
29	seg[62]	42.500	1569.625	
30	seg[63]	42.500	1469.625	

31	seg[64]	42.500	1369.625	
32	seg[65]	42.500	1269.625	
33	seg[66]	42.500	1169.625	
34	seg[67]	42.500	1069.625	
35	seg[68]	42.500	969.625	
36	seg[69]	42.500	869.625	
37	seg[70]	42.500	769.625	
38	seg[71]	42.500	669.625	

Bottom (From Left to Right)				
Pad number	Name	X	Y	Comment
39	VDD5V	639.900	42.500	Double Bond
40	VDD5V	729.900	42.500	Double Bond
41	resetn	819.900	42.500	
42	osc2	909.900	42.500	
43	osc1	999.900	42.500	
44	cl1	1089.900	42.500	
45	cl2	1179.900	42.500	
46	segd	1269.900	42.500	
47	comd	1359.900	42.500	
48	m	1449.900	42.500	
49	rwn	1539.900	42.500	
50	rs	1629.900	42.500	
51	e	1719.900	42.500	
52	tstmd	1809.900	42.500	
53	data[0]	1899.900	42.500	
54	data[1]	1989.900	42.500	
55	data[2]	2079.900	42.500	
56	data[3]	2169.900	42.500	
57	data[4]	2259.900	42.500	
58	data[5]	2349.900	42.500	
59	data[6]	2439.900	42.500	
60	data[7]	2529.900	42.500	
61	VSS	2619.900	42.500	Double Bond
62	VSS	2709.900	42.500	Double Bond
63	vci	2799.900	42.500	
64	c2	2889.900	42.500	
65	c1	2979.900	42.500	
66	vout	3069.900	42.500	
67	VDD	3159.900	42.500	

Right (From Bottom to Top)				
Pad number	Name	X	Y	Comment
68	v5	3595.400	450.000	
69	v4	3595.400	550.000	
70	v3	3595.400	650.000	
71	v2	3595.400	750.000	
72	v1	3595.400	850.000	
73	com[26]	3595.400	950.000	
74	com[25]	3595.400	1050.000	
75	com[24]	3595.400	1150.000	
76	com[23]	3595.400	1250.000	
77	com[22]	3595.400	1350.000	
78	com[21]	3595.400	1450.000	
79	com[20]	3595.400	1550.000	
80	com[19]	3595.400	1650.000	
81	com[18]	3595.400	1750.000	
82	com[17]	3595.400	1850.000	
83	com[16]	3595.400	1950.000	
84	com[15]	3595.400	2050.000	
85	com[14]	3595.400	2150.000	
86	com[13]	3595.400	2250.000	
87	com[12]	3595.400	2350.000	
88	com[11]	3595.400	2450.000	
89	com[10]	3595.400	2550.000	
90	com[9]	3595.400	2650.000	
91	com[8]	3595.400	2750.000	
92	com[7]	3595.400	2850.000	
93	com[6]	3595.400	2950.000	
94	com[5]	3595.400	3050.000	
95	com[4]	3595.400	3150.000	
96	com[3]	3595.400	3250.000	
97	com[2]	3595.400	3350.000	
98	com[1]	3595.400	3450.000	
99	coms	3595.400	3550.000	

100	seg[1]	3595.400	3650.000	
101	seg[2]	3595.400	3750.000	
102	seg[3]	3595.400	3850.000	
103	seg[4]	3595.400	3950.000	
104	seg[5]	3595.400	4050.000	
105	seg[6]	3595.400	4150.000	
106	seg[7]	3595.400	4250.000	

Top (From Right to Left)				
Pad number	Name	X	Y	Comment
107	seg[8]	3075.000	4810.125	
108	seg[9]	2975.000	4810.125	
109	seg[10]	2875.000	4810.125	
110	seg[11]	2775.000	4810.125	
111	seg[12]	2675.000	4810.125	
112	seg[13]	2575.000	4810.125	
113	seg[14]	2475.000	4810.125	
114	seg[15]	2375.000	4810.125	
115	seg[16]	2275.000	4810.125	
116	seg[17]	2175.000	4810.125	
117	seg[18]	2075.000	4810.125	
118	seg[19]	1975.000	4810.125	
119	seg[20]	1875.000	4810.125	
120	seg[21]	1775.000	4810.125	
121	seg[22]	1675.000	4810.125	
122	seg[23]	1575.000	4810.125	
123	seg[24]	1475.000	4810.125	
124	seg[25]	1375.000	4810.125	
125	seg[26]	1275.000	4810.125	
126	seg[27]	1175.000	4810.125	
127	seg[28]	1075.000	4810.125	
128	seg[29]	975.000	4810.125	
129	seg[30]	875.000	4810.125	
130	seg[31]	775.000	4810.125	
131	seg[32]	675.000	4810.125	
132	seg[33]	575.000	4810.125	

Pin Function (XD1602A0)

Table 1 Pin Functional Description

Signal	Number Of Pins	I/O	Device Interfaced with	Function
RESET*	1	I	-	Acts as reset input pin. The LSI is initialized during low level Refer Reset Function. Must be reset after power-on
RS/CS*	1	I	MPU	Select interface mode with the MPU: Low:Serial mode High::Control register(write RAM data(read/write) Acts as chip-select during serial mode; Low: Select(access enable) High: Not selected (access disable)
$\overline{\text{RW}}/\text{SID}$	1	I	MPU	Senlects read/write during bus mode; Low:Write High:Read Input serial data during serial mode.
E/SCLK	1	I	MPU	Starts data read/write during bus mode; Input (Receives) serial clock during serial mode.
DB1 to DB7	7	I/O	MPU	Seven high-order bidirectional tristate data bus pins. Used for data transfer between the MPU and the XD1601A0.DB7 can be used as a busy flag. Open these pins during serial mode since these signals are not used.
DB0/ SOD	1	I/O	MPU	The lowest bidirectional data bit(DB0) during bus Mode .Outputs(transmits)serial data during serial Mode .Open this pin if reading (transmission)is not Performed.
SEG1 to SEG191	191	O	LCD	Display data output signals for the segment extension driver
COMS	1	O	LCD	Acts as a common output signal for segment display Used to display icon and marks beside the character Display
COM1 to COM24	24	O	LCD	Acts as common output signals for character display COM15 to COM24 become non-selective waveforms When the duty ratio is 1/14
COM25/ COMD	1	O	LCD/ Extension driver	Acts as common output signal (COM25)for character Display when EX2 bit is 0. Acts as a common Extension pulse signal(COMD)when EX2 bit is 1. The pin is grounded after RESET input is cleared. When this signal is used as COMD.GND \geq V5 must be maintained.

Table 1 Pin Functional Description (cont. XD1602A0)

Signal	Number of Pins	I/O	Device	Interfaced with Function
CL1	1	O	Extension driver	Outputs the latch pulse of segment extension driver. Can also be used as a shift clock of common extension driver. Enters tristate when both EXT1 and
CL2	1	O	Extension driver	Outputs shift clock of segment extension driver. Can also be used as a common extension driver latch clock. Enters tristate when both EXT1 and EXT2 are 0.
SEGD	1	O	Extension driver	Outputs data of extension driver. Data after the 72nd dot is output. Enters tristate when EXT1 bit is 0
M	1	O	Extension driver	Acts as an alternating current signal of extension driver. Enters tristate when both EXT1 and EXT2 bits are 0.
V1 to V5	5	—	Extension driver	Power supply Power supply for LCD drive $V_{CC} - V5 = 15V$ (max)
V _{CC} /GND	2	—	Power supply	V _{CC} : +2.4V to +5.5V, GND: 0V
OSC1/ OSC2	2	—	Oscillation resistor/ clock	When crystal oscillation is performed, an external resistor must be connected. When the pin input is an external clock, it must be input to OSC1
Vci	1	I	—	— Inputs voltage to the booster to generate the liquid crystal display drive voltage. Vci is reference voltage and power supply for the booster. Vci: $1.0V$ to $5.0V \leq V_{CC}$.
V5OUT2	1	O	V5 pin	Booster capacitor Voltage input to the Vci pin is boosted twice and output. When the voltage is boosted three times, a capacitor with the same capacitance as that of C1–C2 should be connected here.
V5OUT3	1	O	V5 pin	input to the Vci pin is boosted three times and output.
C1/C2	2	—	Booste	capacitor External capacitor should be connected here when using the booster.

Function Description

System Interface

The XD1602A0 have an 8-bit bus.

The XD1602A0 has five types of 8-bit registers: an index register (IDR), status register (STR), various control registers, RAM address register (RAR), and RAM data register (RDR).

The index register (IDR) selects control registers, the RAM address register (RAR) or the RAM data register (RDR) for performing data transfer.

The status register (STR) indicates the internal state of the system. Various control registers store display control data here.

The RAM address register (RAR) stores the address data of display data RAM (DDRAM), character generator RAM (CGRAM), and segment RAM (SEGRAM).

The RAM data register (RDR) temporarily stores data to be written into DDRAM, CGRAM, or SEGRAM. Data written into the RDR from the MPU is automatically written into DDRAM, CGRAM, or SEGRAM by internal operations. The RDR is also used for data storage when reading data from DDRAM, CGRAM, or SEGRAM. Here, when address information is written into the RAR, data is read and then stored into the RDR from DDRAM, CGRAM, or SEGRAM by internal operations.

Data transfer between the MPU is then completed when the MPU reads the RDR. After this read, data in DDRAM, CGRAM, or SEGRAM stored at the next address is sent to the RDR at the next data read from the MPU.

These registers can be selected by the register select signal (RS) and the read/write signal (R/W) in the 8-bit bus interface.

Busy Flag

When the busy flag is 1, the XD1602A0 is in internal operation mode, and only the status register (STR) can be accessed. The busy flag (BF) is output from bit 7 (DB7). Access of other registers can be performed only after confirming that the busy flag is 0.

RAM Address Counter (RAR)

The RAM address counter (RAR) provides addresses for accessing DDRAM, CGRAM, or SEGRAM. When an initial address value is written into the RAM counter (RAR), the RAR is automatically incremented or decremented by 1. Note that a control register specifies which RAM (DDRAM, CGRAM, SEGRAM) to select.

Table 3 Register Selection

RS	R/W	Operation
0	0	IDR write
0	1	STR read
1	0	Control register write, RAM address register (RAR) write, and RAM data register (RDR) write
1	1	RAM data register (RDR) read

Display Data RAM (DDRAM)

Display data RAM (DDRAM) stores character codes and display attribute codes for displaying data. A full-size font is displayed using two bytes, and a half-size font is displayed using one byte. Since the RAM capacity is 80 bytes, 40 full-size characters or 80 half-size characters can be stored.

DDRAM displays only that data stored within the range corresponding to the number of display columns. Data stored outside the range is ignored. Refer to Combined Display of Full-Size and Half-Size characters for details on character codes stored in DDRAM. The relationship between DDRAM addresses and LCD display position depends on the number of display lines (1 line/2 lines/4 lines).

Execution of the display-clear instruction writes H'A0 corresponding to the half-size character for "space" throughout DDRAM.

Note: The XD1602A0 perform display by reading character codes from the DDRAM according to the number of display columns set by the control register. In particular, reading from the DDRAM begins at the position corresponding to the rightmost character as set by the maximum number of display columns. This means that one byte of a two-byte full-size character code should not be set in a position exceeding the maximum number of display columns. For example, do not write a full-size code (2 bytes) in the 12th and 13th byte when the display is set for six characters.

- 2-line display (NL1/0 = 01)

The first line in the DDRAM address is displayed for the 40 bytes of addresses from H'00 to H'27, and the second line is displayed for the 40 bytes of addresses from H'40 to H'67. When there are fewer than 20 display characters (at full size), only the number of display characters specified by NC1/0 will be displayed starting from the leftmost address of the DDRAM. For example, 24 bytes of addresses from H'00 to H'0B and H'40 to H'4B are used when a 6-character display (NC1/0 = 00) is performed using one XD1602A0. Addresses from H'0C and H'4C on are ignored. See Figure 2 for a 2-line display.

Figure 1 1-Line Display (NL1/0 = 00)

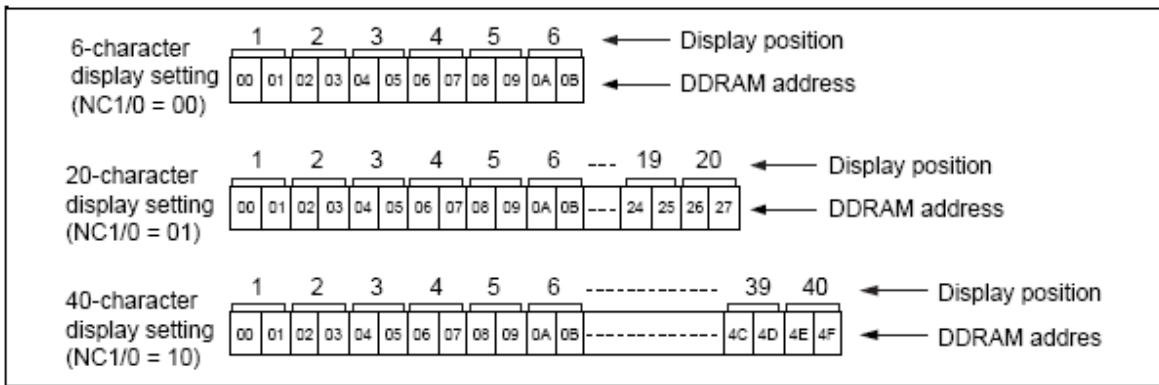
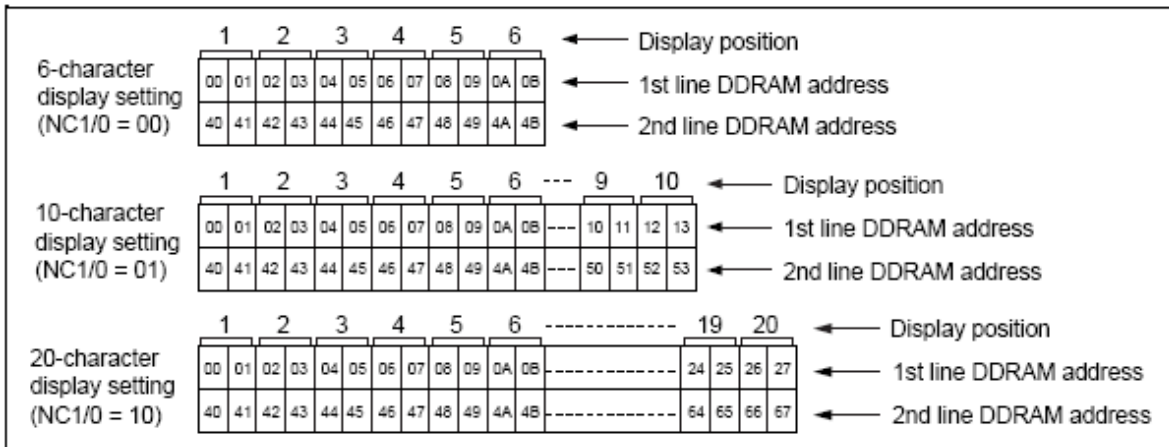


Figure 2 2-Line Display (NL1/0 = 01)



Character Generator ROM for a Full-Size Font (FCGROM)

The character generator ROM for a full-size font (FCGROM) generates 3,840 11×12 dot full-size character patterns from a 12-bit character code. Table 4 shows the relationship between character codes set in DDRAM and full-size font patterns. Refer to Combined Display of Full-Size and Half-Size Characters for the relationship between KSC5601 codes and the character codes to be set in the DDRAM.

Character Generator ROM for a Half-Size Font (HCGROM)

The character generator ROM for a half-size font (HCGROM) generates 128 6×12 dot character patterns from 7-bit character codes. A half-size font (alphanumeric characters and symbols) can be displayed together with a full-size font. Refer to Combined Display of Full-Size and Half-Size Characters for details.

Character Generator RAM (CGRAM)

The character generator RAM (CGRAM) allows the user to display arbitrary full-size font patterns. It can display $8 \times 12 \times 13$ dot fonts.

This RAM can also display double-size characters and figures by combining multiple CGRAM fonts. Specify character codes from H'000 to H'007 in a full size of character code when displaying font patterns stored in the CGRAM.

Segment RAM (SEGRAM)

The segment RAM (SEGRAM) is used to control icons and marks in segment units by the user program. Bits in SEGRAM corresponding to segments to be displayed are directly set by the MPU, regardless of the contents of DDRAM and CGRAM. The SEGRAM is read and displayed when the COMS output pin is selected.

Timing Generator

The timing generator generates timing signals for the operation of internal circuits such as DDRAM, FCGROM, HCGROM, CGRAM, and SEGRAM. RAM read timing for display and internal operation timing for MPU access are generated separately to avoid interference. This prevents undesirable

interferences, such as flickering, in areas other than the display area when writing data to DDRAM, for example.

The timing generator of XD1602A0 generates interface control signals CL1, CL2, M, and COMD-output of extension drivers for a extension configuration.

Display Attribute Controller

The display attribute controller displays white/black inverse, blinking, and white/black inverse blinking for a full size font in FCGROM according to the attribute code set in the DDRAM. Refer to Display Attribute Designation for details.

Fonts in CGRAM and bit patterns in SEGRAM control display attributes using the upper two bits (bits 7 and 6) in each display-pattern data.

Cursor Control Circuit

The cursor control circuit is used to produce a cursor on a displayed character corresponding to the DDRAM address set in the RAM address counter (RAR). Cursors can be chosen from three types: 12th raster-row cursor that is displayed only on the 12th raster-row of each font; blink cursor that periodically displays the whole font in black and white and black inverted cursor that periodically displays the font in white and black (see Figure 9). Note that when the RAM address counter (RAR) is selecting CGRAM or SEGRAM, a cursor would be generated at that address, however, it does not have any meaning.

Note: One display line consists of 13 raster-rows.

Smooth Scroll Control Circuit

The smooth scroll control circuit is used to perform a smooth-scroll in units of dots.

When the number of characters to be displayed is greater than that possible at one time in the liquid crystal module, this horizontal smooth scroll can be used to display characters in an easy-to-read manner for each line. Refer to Horizontal Smooth Scroll for details for each line.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit of XD1602A0 consists of 26 common signal drivers and 191 segment signal drivers. When the liquidcrystal driver duty ratio is set by a program, the necessary common signal drivers output drive waveforms and the remaining common drivers output non-selected waveforms. In addition, drivers can be expanded on the common and segment sides through register settings.

Display pattern data is sent serially through a shift register and latched when all needed data has arrived. The latched data then enables the LCD driver to generate drive waveform outputs. This serial data is sent from the display pattern that corresponds to the last address of the DDRAM and is latched when the character pattern of the display data corresponding to the first address enters the internal shift register.

Booster

The booster outputs a voltage that is two or three times higher than the reference voltage input from pin Vci. Since the LCD voltage can be generated from the LSI operation power supply, this circuit can operate with a single power supply. Refer to Power Supply for Liquid Crystal Display Drive for details.

Oscillator

The XD1602A0 performs R-C oscillation by adding a single external oscillation resistor. The oscillation frequency corresponding to display size and frame frequency can be adjusted by changing the oscillation resistor. Refer to Oscillator for details.

Table 6 Relationship between Half-Size Character Code and Character Pattern
(ROM Code: A00)

Upper (4 bits) Lower (3 bits)	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 000	0	1	2	(Space)	3	4	5	6	7	8	9	0	A	B	C	D
xxxx 001	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T
xxxx 010	U	V	W	X	Y	Z	[\]	^	_	`	{		}	~
xxxx 011	!	"	#	\$	%	&	'	()	*	+	=	<	>	?	@
xxxx 100	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~
xxxx 101	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~
xxxx 110	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~
xxxx 111	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~	~

XD1602A0 Korean font set (KS C 5601-1992 subset) – Half Font

f	ㄱ	ㅋ	ㄴ	ㄷ	ㄹ	ㅁ	ㅂ
e	ㅅ	ㅆ	ㅇ	ㅈ	ㅊ	ㅌ	ㅍ
d	ㅊ	ㅋ	ㆁ	ㆁ	ㆁ	ㆁ	ㆁ
c	ㅊ	ㅋ	ㆁ	ㆁ	ㆁ	ㆁ	ㆁ
b	ㅊ	ㅋ	ㆁ	ㆁ	ㆁ	ㆁ	ㆁ
a	ㅊ	ㅋ	ㆁ	ㆁ	ㆁ	ㆁ	ㆁ
9	ㅊ	ㅋ	ㆁ	ㆁ	ㆁ	ㆁ	ㆁ
8	ㅊ	ㅋ	ㆁ	ㆁ	ㆁ	ㆁ	ㆁ
7	ㅊ	ㅋ	ㆁ	ㆁ	ㆁ	ㆁ	ㆁ
6	ㅊ	ㅋ	ㆁ	ㆁ	ㆁ	ㆁ	ㆁ
5	ㅊ	ㅋ	ㆁ	ㆁ	ㆁ	ㆁ	ㆁ
4	ㅊ	ㅋ	ㆁ	ㆁ	ㆁ	ㆁ	ㆁ
3	ㅊ	ㅋ	ㆁ	ㆁ	ㆁ	ㆁ	ㆁ
2	ㅊ	ㅋ	ㆁ	ㆁ	ㆁ	ㆁ	ㆁ
1	ㅊ	ㅋ	ㆁ	ㆁ	ㆁ	ㆁ	ㆁ
0	ㅊ	ㅋ	ㆁ	ㆁ	ㆁ	ㆁ	ㆁ
0x000	0x010	0x020	0x030	0x040	0x050	0x060	0x070

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (3)

	0	1	2	3	4	5	6	7	8	9	a	b	c	d	e	f
0x100	ㄱ	ㅋ	ㆁ	ㄴ	ㄷ	ㄹ	ㅁ	ㅂ	ㅅ	ㅇ	ㅈ	ㅊ	ㅌ	ㅍ	ㅑ	ㅓ
0x110	ㅕ	ㅖ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅣ	ㅍ	ㅑ	ㅓ	ㅕ	ㅖ	ㅗ	ㅛ	ㅜ
0x120	ㅠ	ㅡ	ㅣ	ㅍ	ㅑ	ㅓ	ㅕ	ㅖ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅣ	ㅍ	ㅑ
0x130	ㅓ	ㅕ	ㅖ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅣ	ㅍ	ㅑ	ㅓ	ㅕ	ㅖ	ㅗ	ㅛ
0x140	ㅜ	ㅠ	ㅡ	ㅣ	ㅍ	ㅑ	ㅓ	ㅕ	ㅖ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅣ	ㅍ
0x150	ㅑ	ㅓ	ㅕ	ㅖ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅣ	ㅍ	ㅑ	ㅓ	ㅕ	ㅖ	ㅗ
0x160	ㅛ	ㅜ	ㅠ	ㅡ	ㅣ	ㅍ	ㅑ	ㅓ	ㅕ	ㅖ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅣ
0x170	ㅝ	ㅞ	ㅟ	ㅠ	ㅡ	ㅢ	ㅣ	ㅤ	ㅥ	ㅦ	ㅧ	ㅨ	ㅩ	ㅪ	ㅫ	ㅬ

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (4)

	f						
	e						
	d						
	c						
	b						
	a						
	9						
	8						
	7						
	6						
	5						
	4						
	3						
	2						
	1						
	0						
0x180							
0x190							
0x1a0							
0x1b0							
0x1c0							
0x1d0							
0x1e0							
0x1f0							

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (6)

	f	아	안	어	어	어	어
	e	우	우	우	우	우	우
	d	이	이	이	이	이	이
	c	이	이	이	이	이	이
	b	아	아	아	아	아	아
	a	아	아	아	아	아	아
	9	아	아	아	아	아	아
	8	아	아	아	아	아	아
	7	아	아	아	아	아	아
	6	아	아	아	아	아	아
	5	아	아	아	아	아	아
	4	아	아	아	아	아	아
	3	아	아	아	아	아	아
	2	아	아	아	아	아	아
	1	아	아	아	아	아	아
	0	아	아	아	아	아	아
0x280							
0x290							
0x2a0							
0x2b0							
0x2c0							
0x2d0							
0x2e0							
0x2f0							

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (7)

f	ㅍ	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅝ
e	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅝ	ㅟ
d	ㅓ	ㅕ	ㅗ	ㅛ	ㅝ	ㅟ	ㅡ
c	ㅕ	ㅗ	ㅛ	ㅝ	ㅟ	ㅡ	ㅣ
b	ㅗ	ㅛ	ㅝ	ㅟ	ㅡ	ㅣ	ㅥ
a	ㅛ	ㅝ	ㅟ	ㅡ	ㅣ	ㅥ	ㅧ
9	ㅝ	ㅟ	ㅡ	ㅣ	ㅥ	ㅧ	ㅩ
8	ㅟ	ㅡ	ㅣ	ㅥ	ㅧ	ㅩ	ㅫ
7	ㅡ	ㅣ	ㅥ	ㅧ	ㅩ	ㅫ	ㅭ
6	ㅣ	ㅥ	ㅧ	ㅩ	ㅫ	ㅭ	ㅯ
5	ㅥ	ㅧ	ㅩ	ㅫ	ㅭ	ㅯ	ㅱ
4	ㅧ	ㅩ	ㅫ	ㅭ	ㅯ	ㅱ	ㅳ
3	ㅩ	ㅫ	ㅭ	ㅯ	ㅱ	ㅳ	ㅵ
2	ㅫ	ㅭ	ㅯ	ㅱ	ㅳ	ㅵ	ㅷ
1	ㅭ	ㅯ	ㅱ	ㅳ	ㅵ	ㅷ	ㅹ
0	ㅯ	ㅱ	ㅳ	ㅵ	ㅷ	ㅹ	ㅻ
0x300	0x310	0x320	0x330	0x340	0x350	0x360	0x370

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (8)

0	A	B	Г	Д	Е	Ё	Ж	З	И	Й	К	Л	М	Н	О
1	П	Р	С	Т	У	Ф	Х	Ц	Ч	Ш	Щ	Ъ	Ы	Ь	Э
2	Ю	Я													
3	А	Б	Г	Д	Е	Ё	Ж	З	И	Й	К	Л	М	Н	О
4	П	Р	С	Т	У	Ф	Х	Ц	Ч	Ш	Щ	Ъ	Ы	Ь	Э
5	Ю	Я													
6															
7															
8															
9															
a															
b															
c															
d															
e															
f															
0x380															
0x390															
0x3a0															
0x3b0															
0x3c0															
0x3d0															
0x3e0															
0x3f0															

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (9)

f	ㄴ	ㄷ	ㄹ	ㅁ	ㅂ	ㅅ	ㅇ	
e	ㄴ	ㄷ	ㄹ	ㅁ	ㅂ	ㅅ	ㅇ	
d	ㄴ	ㄷ	ㄹ	ㅁ	ㅂ	ㅅ	ㅇ	
c	ㄴ	ㄷ	ㄹ	ㅁ	ㅂ	ㅅ	ㅇ	
b	ㄴ	ㄷ	ㄹ	ㅁ	ㅂ	ㅅ	ㅇ	
a	ㄴ	ㄷ	ㄹ	ㅁ	ㅂ	ㅅ	ㅇ	
9	ㄴ	ㄷ	ㄹ	ㅁ	ㅂ	ㅅ	ㅇ	
8	ㄴ	ㄷ	ㄹ	ㅁ	ㅂ	ㅅ	ㅇ	
7	ㄴ	ㄷ	ㄹ	ㅁ	ㅂ	ㅅ	ㅇ	
6	ㄴ	ㄷ	ㄹ	ㅁ	ㅂ	ㅅ	ㅇ	
5	ㄴ	ㄷ	ㄹ	ㅁ	ㅂ	ㅅ	ㅇ	
4	ㄴ	ㄷ	ㄹ	ㅁ	ㅂ	ㅅ	ㅇ	
3	ㄴ	ㄷ	ㄹ	ㅁ	ㅂ	ㅅ	ㅇ	
2	ㄴ	ㄷ	ㄹ	ㅁ	ㅂ	ㅅ	ㅇ	
1	ㄴ	ㄷ	ㄹ	ㅁ	ㅂ	ㅅ	ㅇ	
0	ㄴ	ㄷ	ㄹ	ㅁ	ㅂ	ㅅ	ㅇ	
	0x400	0x410	0x420	0x430	0x440	0x450	0x460	0x470

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (10)

f	과	나	라	로	리	와	요	우
e	하	가	라	로	리	와	요	우
d	하	가	라	로	리	와	요	우
c	하	가	라	로	리	와	요	우
b	하	가	라	로	리	와	요	우
a	하	가	라	로	리	와	요	우
9	하	가	라	로	리	와	요	우
8	하	가	라	로	리	와	요	우
7	하	가	라	로	리	와	요	우
6	하	가	라	로	리	와	요	우
5	하	가	라	로	리	와	요	우
4	하	가	라	로	리	와	요	우
3	하	가	라	로	리	와	요	우
2	하	가	라	로	리	와	요	우
1	하	가	라	로	리	와	요	우
0	하	가	라	로	리	와	요	우
	0x480	0x490	0x4a0	0x4b0	0x4c0	0x4d0	0x4e0	0x4f0

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (11)

f	ㅍ	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	
e	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	
d	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	
c	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	
b	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	
a	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	
9	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	
8	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	
7	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	
6	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	
5	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	
4	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	
3	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	
2	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	
1	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	
0	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	
	0x500	0x510	0x520	0x530	0x540	0x550	0x560	0x570

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (12)

f	ㅍ	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ
e	ㅍ	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ
d	ㅍ	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ
c	ㅍ	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ
b	ㅍ	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ
a	ㅍ	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ
9	ㅍ	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ
8	ㅍ	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ
7	ㅍ	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ
6	ㅍ	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ
5	ㅍ	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ
4	ㅍ	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ
3	ㅍ	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ
2	ㅍ	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ
1	ㅍ	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ
0	ㅍ	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ
	0x580	0x590	0x5a0	0x5b0	0x5c0	0x5d0	0x5e0	0x5f0

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (13)

f	ㅍ	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅝ	ㅞ	ㅟ
e	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅝ	ㅞ	ㅟ	ㅠ
d	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅝ	ㅞ	ㅟ	ㅡ
c	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅝ	ㅞ	ㅟ	ㅢ
b	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅝ	ㅞ	ㅟ	ㅣ
a	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅝ	ㅞ	ㅟ	ㅤ
9	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅝ	ㅞ	ㅟ	ㅥ
8	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅝ	ㅞ	ㅟ	ㅦ
7	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅝ	ㅞ	ㅟ	ㅧ
6	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅝ	ㅞ	ㅟ	ㅨ
5	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅝ	ㅞ	ㅟ	ㅩ
4	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅝ	ㅞ	ㅟ	ㅪ
3	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅝ	ㅞ	ㅟ	ㅫ
2	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅝ	ㅞ	ㅟ	ㅬ
1	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅝ	ㅞ	ㅟ	ㅭ
0	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅝ	ㅞ	ㅟ	ㅮ
	0x600	0x610	0x620	0x630	0x640	0x650	0x660	0x670				

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (14)

f	ㄱ	ㄴ	ㄷ	ㄹ	ㅁ	ㅂ	ㅃ	ㅄ
e	ㅅ	ㅇ	ㅈ	ㅊ	ㅋ	ㆁ	ㆂ	ㆃ
d	ㆄ	ㆅ	ㆆ	ㆇ	ㆈ	ㆉ	ㆊ	ㆋ
c	ㆌ	ㆍ	ㆎ	㆏	㆐	㆑	㆒	㆓
b	㆕	㆖	㆗	㆘	㆙	㆚	㆛	㆜
a	㆝	㆞	㆟	ㆠ	ㆡ	ㆢ	ㆣ	ㆤ
9	ㆥ	ㆦ	ㆧ	ㆨ	ㆩ	ㆪ	ㆫ	ㆬ
8	ㆭ	ㆮ	ㆯ	ㆰ	ㆱ	ㆲ	ㆳ	ㆴ
7	ㆵ	ㆶ	ㆷ	ㆸ	ㆹ	ㆺ	ㆻ	ㆼ
6	ㆽ	ㆿ	ㆾ	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ
5	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ
4	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ
3	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ
2	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ
1	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ
0	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ	ㆿ
	0x680	0x690	0x6a0	0x6b0	0x6c0	0x6d0	0x6e0	0x6f0

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (15)

f	하<하	하	하	하	하	하	하	하
e	하	하	하	하	하	하	하	하
d	하	하	하	하	하	하	하	하
c	하	하	하	하	하	하	하	하
b	하	하	하	하	하	하	하	하
a	하	하	하	하	하	하	하	하
9	하	하	하	하	하	하	하	하
8	하	하	하	하	하	하	하	하
7	하	하	하	하	하	하	하	하
6	하	하	하	하	하	하	하	하
5	하	하	하	하	하	하	하	하
4	하	하	하	하	하	하	하	하
3	하	하	하	하	하	하	하	하
2	하	하	하	하	하	하	하	하
1	하	하	하	하	하	하	하	하
0	하	하	하	하	하	하	하	하
	0x700	0x710	0x720	0x730	0x740	0x750	0x760	0x770

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (16)

f	꺃	꺃	꺃	꺃	꺃	꺃	꺃	
e	꺃	꺃	꺃	꺃	꺃	꺃	꺃	
d	꺃	꺃	꺃	꺃	꺃	꺃	꺃	
c	꺃	꺃	꺃	꺃	꺃	꺃	꺃	
b	꺃	꺃	꺃	꺃	꺃	꺃	꺃	
a	꺃	꺃	꺃	꺃	꺃	꺃	꺃	
9	꺃	꺃	꺃	꺃	꺃	꺃	꺃	
8	꺃	꺃	꺃	꺃	꺃	꺃	꺃	
7	꺃	꺃	꺃	꺃	꺃	꺃	꺃	
6	꺃	꺃	꺃	꺃	꺃	꺃	꺃	
5	꺃	꺃	꺃	꺃	꺃	꺃	꺃	
4	꺃	꺃	꺃	꺃	꺃	꺃	꺃	
3	꺃	꺃	꺃	꺃	꺃	꺃	꺃	
2	꺃	꺃	꺃	꺃	꺃	꺃	꺃	
1	꺃	꺃	꺃	꺃	꺃	꺃	꺃	
0	꺃	꺃	꺃	꺃	꺃	꺃	꺃	
	0x780	0x790	0x7a0	0x7b0	0x7c0	0x7d0	0x7e0	0x7f0

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (17)

f	ㅍ	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	
e	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	
d	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	
c	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅣ	
b	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅣ	ㅍ	
a	ㅛ	ㅜ	ㅠ	ㅡ	ㅣ	ㅍ	ㅑ	
9	ㅜ	ㅠ	ㅡ	ㅣ	ㅍ	ㅑ	ㅓ	
8	ㅠ	ㅡ	ㅣ	ㅍ	ㅑ	ㅓ	ㅕ	
7	ㅡ	ㅣ	ㅍ	ㅑ	ㅓ	ㅕ	ㅗ	
6	ㅣ	ㅍ	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	
5	ㅍ	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	
4	ㅑ	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	
3	ㅓ	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	
2	ㅕ	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅣ	
1	ㅗ	ㅛ	ㅜ	ㅠ	ㅡ	ㅣ	ㅍ	
0	ㅛ	ㅜ	ㅠ	ㅡ	ㅣ	ㅍ	ㅑ	
	0x800	0x810	0x820	0x830	0x840	0x850	0x860	0x870

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (18)

f	예	에	어	이	의	이	의	의
e	예	에	어	이	의	이	의	의
d	예	에	어	이	의	이	의	의
c	예	에	어	이	의	이	의	의
b	예	에	어	이	의	이	의	의
a	예	에	어	이	의	이	의	의
9	예	에	어	이	의	이	의	의
8	예	에	어	이	의	이	의	의
7	예	에	어	이	의	이	의	의
6	예	에	어	이	의	이	의	의
5	예	에	어	이	의	이	의	의
4	예	에	어	이	의	이	의	의
3	예	에	어	이	의	이	의	의
2	예	에	어	이	의	이	의	의
1	예	에	어	이	의	이	의	의
0	예	에	어	이	의	이	의	의
	0x880	0x890	0x8a0	0x8b0	0x8c0	0x8d0	0x8e0	0x8f0

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (19)

f	해	해	해	해	해	해	해	
e	해	해	해	해	해	해	해	
d	해	해	해	해	해	해	해	
c	해	해	해	해	해	해	해	
b	해	해	해	해	해	해	해	
a	해	해	해	해	해	해	해	
9	해	해	해	해	해	해	해	
8	해	해	해	해	해	해	해	
7	해	해	해	해	해	해	해	
6	해	해	해	해	해	해	해	
5	해	해	해	해	해	해	해	
4	해	해	해	해	해	해	해	
3	해	해	해	해	해	해	해	
2	해	해	해	해	해	해	해	
1	해	해	해	해	해	해	해	
0	해	해	해	해	해	해	해	
	0x900	0x910	0x920	0x930	0x940	0x950	0x960	0x970

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (20)

f	ㅈ	ㅊ	ㅋ	ㆁ	ㆂ	ㆃ	ㆄ	
e	ㅅ	ㅆ	ㅇ	ㆁ	ㆂ	ㆃ	ㆄ	
d	ㅈ	ㅊ	ㅋ	ㆁ	ㆂ	ㆃ	ㆄ	
c	ㅅ	ㅆ	ㅇ	ㆁ	ㆂ	ㆃ	ㆄ	
b	ㅈ	ㅊ	ㅋ	ㆁ	ㆂ	ㆃ	ㆄ	
a	ㅅ	ㅆ	ㅇ	ㆁ	ㆂ	ㆃ	ㆄ	
9	ㅈ	ㅊ	ㅋ	ㆁ	ㆂ	ㆃ	ㆄ	
8	ㅅ	ㅆ	ㅇ	ㆁ	ㆂ	ㆃ	ㆄ	
7	ㅈ	ㅊ	ㅋ	ㆁ	ㆂ	ㆃ	ㆄ	
6	ㅅ	ㅆ	ㅇ	ㆁ	ㆂ	ㆃ	ㆄ	
5	ㅈ	ㅊ	ㅋ	ㆁ	ㆂ	ㆃ	ㆄ	
4	ㅅ	ㅆ	ㅇ	ㆁ	ㆂ	ㆃ	ㆄ	
3	ㅈ	ㅊ	ㅋ	ㆁ	ㆂ	ㆃ	ㆄ	
2	ㅅ	ㅆ	ㅇ	ㆁ	ㆂ	ㆃ	ㆄ	
1	ㅈ	ㅊ	ㅋ	ㆁ	ㆂ	ㆃ	ㆄ	
0	ㅅ	ㅆ	ㅇ	ㆁ	ㆂ	ㆃ	ㆄ	
	0x980	0x990	0x9a0	0x9b0	0x9c0	0x9d0	0x9e0	0x9f0

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (21)

f	꺆	꺇	꺈	꺉	꺊	꺋	꺌	
e	꺍	꺎	꺏	꺐	꺑	꺒	꺓	
d	꺔	꺕	꺖	꺗	꺘	꺙	꺚	
c	꺛	꺜	꺝	꺞	꺟	꺠	꺡	
b	꺢	꺣	꺤	꺥	꺦	꺧	꺨	
a	꺩	꺪	꺫	꺬	꺭	꺮	꺯	
9	꺰	꺱	꺲	꺳	꺴	꺵	꺶	
8	꺷	꺸	꺹	꺺	꺻	꺼	꺽	
7	꺾	꺿	껀	껁	껂	껃	껄	
6	껅	껆	껇	껈	껉	껊	껋	
5	껌	껍	껎	껏	껐	껑	껒	
4	껓	껔	껕	껖	껗	께	껙	
3	껚	껛	껜	껝	껞	껟	껠	
2	껡	껢	껣	껤	껥	껦	껧	
1	껨	껩	껪	껫	껬	껭	껮	
0	껯	껰	껱	껲	껳	껴	껵	
	0xa00	0xa10	0xa20	0xa30	0xa40	0xa50	0xa60	0xa70

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (22)

f	키	키	키	키	키	키	키	
e	키	키	키	키	키	키	키	
d	키	키	키	키	키	키	키	
c	키	키	키	키	키	키	키	
b	키	키	키	키	키	키	키	
a	키	키	키	키	키	키	키	
9	키	키	키	키	키	키	키	
8	키	키	키	키	키	키	키	
7	키	키	키	키	키	키	키	
6	키	키	키	키	키	키	키	
5	키	키	키	키	키	키	키	
4	키	키	키	키	키	키	키	
3	키	키	키	키	키	키	키	
2	키	키	키	키	키	키	키	
1	키	키	키	키	키	키	키	
0	키	키	키	키	키	키	키	
	0xa80	0xa90	0xaa0	0xab0	0xac0	0xad0	0xae0	0xaf0

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (23)

f	과	과	과	과	과	과	과	
e	과	과	과	과	과	과	과	
d	과	과	과	과	과	과	과	
c	과	과	과	과	과	과	과	
b	과	과	과	과	과	과	과	
a	과	과	과	과	과	과	과	
9	과	과	과	과	과	과	과	
8	과	과	과	과	과	과	과	
7	과	과	과	과	과	과	과	
6	과	과	과	과	과	과	과	
5	과	과	과	과	과	과	과	
4	과	과	과	과	과	과	과	
3	과	과	과	과	과	과	과	
2	과	과	과	과	과	과	과	
1	과	과	과	과	과	과	과	
0	과	과	과	과	과	과	과	
	0xb00	0xb10	0xb20	0xb30	0xb40	0xb50	0xb60	0xb70

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (24)

f	과	과	과	과	과	과	과	
e	과	과	과	과	과	과	과	
d	과	과	과	과	과	과	과	
c	과	과	과	과	과	과	과	
b	과	과	과	과	과	과	과	
a	과	과	과	과	과	과	과	
9	과	과	과	과	과	과	과	
8	과	과	과	과	과	과	과	
7	과	과	과	과	과	과	과	
6	과	과	과	과	과	과	과	
5	과	과	과	과	과	과	과	
4	과	과	과	과	과	과	과	
3	과	과	과	과	과	과	과	
2	과	과	과	과	과	과	과	
1	과	과	과	과	과	과	과	
0	과	과	과	과	과	과	과	
	0xb80	0xb90	0xba0	0xbb0	0xbc0	0xbd0	0xbe0	0xbf0

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (25)

f	ㅁ	ㅂ	ㅅ	ㅈ	ㅊ	ㅋ	ㆁ	
e	ㅁ	ㅂ	ㅅ	ㅈ	ㅊ	ㅋ	ㆁ	
d	ㅁ	ㅂ	ㅅ	ㅈ	ㅊ	ㅋ	ㆁ	
c	ㅁ	ㅂ	ㅅ	ㅈ	ㅊ	ㅋ	ㆁ	
b	ㅁ	ㅂ	ㅅ	ㅈ	ㅊ	ㅋ	ㆁ	
a	ㅁ	ㅂ	ㅅ	ㅈ	ㅊ	ㅋ	ㆁ	
9	ㅁ	ㅂ	ㅅ	ㅈ	ㅊ	ㅋ	ㆁ	
8	ㅁ	ㅂ	ㅅ	ㅈ	ㅊ	ㅋ	ㆁ	
7	ㅁ	ㅂ	ㅅ	ㅈ	ㅊ	ㅋ	ㆁ	
6	ㅁ	ㅂ	ㅅ	ㅈ	ㅊ	ㅋ	ㆁ	
5	ㅁ	ㅂ	ㅅ	ㅈ	ㅊ	ㅋ	ㆁ	
4	ㅁ	ㅂ	ㅅ	ㅈ	ㅊ	ㅋ	ㆁ	
3	ㅁ	ㅂ	ㅅ	ㅈ	ㅊ	ㅋ	ㆁ	
2	ㅁ	ㅂ	ㅅ	ㅈ	ㅊ	ㅋ	ㆁ	
1	ㅁ	ㅂ	ㅅ	ㅈ	ㅊ	ㅋ	ㆁ	
0	ㅁ	ㅂ	ㅅ	ㅈ	ㅊ	ㅋ	ㆁ	
	0xc00	0xc10	0xc20	0xc30	0xc40	0xc50	0xc60	0xc70

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (26)

f	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	
e	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	
d	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	
c	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	
b	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	
a	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	
9	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	
8	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	
7	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	
6	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	
5	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	
4	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	
3	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	
2	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	
1	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	
0	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	ㅅ	
	0xc80	0xc90	0xca0	0xcb0	0xcc0	0xcd0	0xce0	0xcf0

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (27)

f	ㅅ	ㅆ	=	ㄴ	ㄹ	ㅁ	ㅂ
e	ㅈ	ㅊ	ㅡ	ㅣ	ㅅ	ㅈ	ㅊ
d	ㅊ	ㅌ	ㅍ	ㅇ	㉿	ㅍ	ㅑ
c	ㅊ	ㅌ	ㅍ	ㄷ	ㅍ	ㅑ	ㅓ
b	ㅊ	ㅌ	ㅍ	ㅂ	ㅍ	ㅑ	ㅓ
a	ㅊ	ㅌ	ㅍ	ㅂ	ㅍ	ㅑ	ㅓ
9	ㅊ	ㅌ	ㅍ	ㅂ	ㅍ	ㅑ	ㅓ
8	ㅊ	ㅌ	ㅍ	ㅂ	ㅍ	ㅑ	ㅓ
7	ㅊ	ㅌ	ㅍ	ㅂ	ㅍ	ㅑ	ㅓ
6	ㅊ	ㅌ	ㅍ	ㅂ	ㅍ	ㅑ	ㅓ
5	ㅊ	ㅌ	ㅍ	ㅂ	ㅍ	ㅑ	ㅓ
4	ㅊ	ㅌ	ㅍ	ㅂ	ㅍ	ㅑ	ㅓ
3	ㅊ	ㅌ	ㅍ	ㅂ	ㅍ	ㅑ	ㅓ
2	ㅊ	ㅌ	ㅍ	ㅂ	ㅍ	ㅑ	ㅓ
1	ㅊ	ㅌ	ㅍ	ㅂ	ㅍ	ㅑ	ㅓ
0	ㅊ	ㅌ	ㅍ	ㅂ	ㅍ	ㅑ	ㅓ
	0xd00	0xd10	0xd20	0xd30	0xd40	0xd50	0xd60
							0xd70

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (28)

f	\$	4	D	T	d	·	·
e	#	3	O	S	o	s	·
d	*	2	B	R	b	r	·
c	!	1	A	Q	a	q	·
b	_	0	@	P	_	p	·
a	{	/	?	N	o	n	■
9		.	>	M	m		
8	{	-	=	L	l	}	
7	z	~	<	K	k		
6	y	+	:	J	j		E
5	x	*	:	I	i	z	v
4	w)	9	H	h	x	s
3	v	(8	G	g	x	%
2	u	,	7	F	f	w	·
1	t	&	6	E	e	v	+
0	s	%	5	D	d	u	+
0xd80	0xd90	0xda0	0xdb0	0xdc0	0xdd0	0xde0	0xdf0

XD1602A0 Korean font set (KS C 5601-1992 subset) – Full Font (30)

f	⦿	⦿	⦿	⦿	⦿	⦿	⦿
e	⦿	⦿	⦿	⦿	⦿	⦿	⦿
d	⦿	⦿	⦿	⦿	⦿	⦿	⦿
c	⦿	⦿	⦿	⦿	⦿	⦿	⦿
b	⦿	⦿	⦿	⦿	⦿	⦿	⦿
a	⦿	⦿	⦿	⦿	⦿	⦿	⦿
9	⦿	⦿	⦿	⦿	⦿	⦿	⦿
8	⦿	⦿	⦿	⦿	⦿	⦿	⦿
7	⦿	⦿	⦿	⦿	⦿	⦿	⦿
6	⦿	⦿	⦿	⦿	⦿	⦿	⦿
5	⦿	⦿	⦿	⦿	⦿	⦿	⦿
4	⦿	⦿	⦿	⦿	⦿	⦿	⦿
3	⦿	⦿	⦿	⦿	⦿	⦿	⦿
2	⦿	⦿	⦿	⦿	⦿	⦿	⦿
1	⦿	⦿	⦿	⦿	⦿	⦿	⦿
0	⦿	⦿	⦿	⦿	⦿	⦿	⦿
	0xe80	0xe90	0xea0	0xeb0	0xec0	0xed0	0xee0
	0xef0						

Notes: 1. CGRAM is selected when the upper 9 bits (C3 to C11) of the full size character codes are 0. in this case, the lower 3 bits (C0 to C2) of the character code correspond to bits 5 to 7 (A5 to A7) (3bits : 8types) in the CGRAM address.

2. CGRAM address bits 1 to 4 (A1 to A4) designate the character pattern line position. The 12th line is the cursor position and its display is formed by a logical OR with the cursor.

3. CGRAM address 0 (A0) corresponds to the left-half and right-half of a full-size character pattern.

4. The character data is stored with the rightmost character element in bit 0 (LSB), as shown in the table above. Pattern produced by bits 0 to 5 is displayed and 13 raster-rows are displayed together. Thus, an arbitrary character pattern consisting of 12×13 dots can be displayed.

5. A set bit in the CGRAM data corresponds to display selection, and 0 to non-selection.

6. The upper two bits (AA) of CGRAM data indicate the display attribute for the lower 6-bit pattern. In this case, display attributes specified for the DDRAM during full-size character display is disabled. When these upper two bits are 00, the CGRAM pattern is simply displayed as set; when 01, the pattern reverses (black/white), when 10, the pattern blinks; and when 11, the pattern reverses and blinks.

Relationship between SEGRAM Addresses and Display Patterns

SEGRAM data is displayed when the select level of the COMS pin is output. Since SEGRAM data does not depend on character code data in DDRAM, and does not undergo horizontal smooth scroll, it can be used to display icon and marks. The following shows the relationship between SEGRAM addresses and segment output pins.

Table 8 Relationship between SEGRAM Addresses and Display Patterns

SEGRAM Address					SEGRAM Data							
A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	B1	B0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6
0	0	0	0	1	B1	B0	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12
0	0	0	1	0	B1	B0	SEG13	SEG14	SEG15	SEG16	SEG17	SEG18
0	0	0	1	1	B1	B0	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24
0	0	1	0	0	B1	B0	SEG25	SEG26	SEG27	SEG28	SEG29	SEG30
0	0	1	0	1	B1	B0	SEG31	SEG32	SEG33	SEG34	SEG35	SEG36
0	0	1	1	0	B1	B0	SEG37	SEG38	SEG39	SEG40	SEG41	SEG42
0	0	1	1	1	B1	B0	SEG43	SEG44	SEG45	SEG46	SEG47	SEG48
0	1	0	0	0	B1	B0	SEG49	SEG50	SEG51	SEG52	SEG53	SEG54
0	1	0	0	1	B1	B0	SEG55	SEG56	SEG57	SEG58	SEG59	SEG60
0	1	0	1	0	B1	B0	SEG61	SEG62	SEG63	SEG64	SEG65	SEG66
0	1	0	1	1	B1	B0	SEG67	SEG68	SEG69	SEG70	SEG71	SEG72
0	1	1	0	0	B1	B0	SEG73	SEG74	SEG75	SEG76	SEG77	SEG78
0	1	1	0	1	B1	B0	SEG79	SEG80	SEG81	SEG82	SEG83	SEG84
0	1	1	1	0	B1	B0	SEG85	SEG86	SEG87	SEG88	SEG89	SEG90
0	1	1	1	1	B1	B0	SEG91	SEG92	SEG93	SEG94	SEG95	SEG96
1	0	0	0	0	B1	B0	SEG97	SEG98	SEG99	SEG100	SEG101	SEG102
1	0	0	0	1	B1	B0	SEG103	SEG104	SEG105	SEG106	SEG107	SEG108
1	0	0	1	0	B1	B0	SEG109	SEG110	SEG111	SEG112	SEG113	SEG114
1	0	0	1	1	B1	B0	SEG115	SEG116	SEG117	SEG118	SEG119	SEG120
1	0	1	0	0	B1	B0	SEG121	SEG122	SEG123	SEG124	SEG125	SEG126
1	0	1	0	1	B1	B0	SEG127	SEG128	SEG129	SEG130	SEG131	SEG132
1	0	1	1	0	B1	B0	SEG133	SEG134	SEG135	SEG136	SEG137	SEG138
1	0	1	1	1	B1	B0	SEG139	SEG140	SEG141	SEG142	SEG143	SEG144
1	1	0	0	0	B1	B0	SEG145	SEG146	SEG147	SEG148	SEG149	SEG150
1	1	0	0	1	B1	B0	SEG151	SEG152	SEG153	SEG154	SEG155	SEG156
1	1	0	1	0	B1	B0	SEG157	SEG158	SEG159	SEG160	SEG161	SEG162
1	1	0	1	1	B1	B0	SEG163	SEG164	SEG165	SEG166	SEG167	SEG168
1	1	1	0	0	B1	B0	SEG169	SEG170	SEG171	SEG172	SEG173	SEG174
1	1	1	0	1	B1	B0	SEG175	SEG176	SEG177	SEG178	SEG179	SEG180
1	1	1	1	0	B1	B0	SEG181	SEG182	SEG183	SEG184	SEG185	SEG186
1	1	1	1	1	B1	B0	SEG187	SEG188	SEG189	SEG190	SEG191	SEG192

Blinking control

Pattern on/off

Notes: 1. SEG1 to SEG191 are pin numbers of the segment output driver of the XD1602A0. Pin SEG1 is positioned on the left edge of the display.

2. The lower six bits (D0 to D5) indicate display on/off for of each segment. A bit setting of 1 selects display while 0 selects no display.

3. Pattern blinking of the lower six bits is controlled by the upper two bits (D6 and D7) of SEGRAM data. When the upper two bits (B0 and B1) are 10, segments whose corresponding bits in the lower 6 bits are set to 1 will blink on the display. When the upper two bits (B0 and B1) are 01, only the bit-5 pattern can blink. Do not attempt to set the upper two bits (B0 and B1) to 11 (setting is prohibited).

Register Functions

Outline

Data can be written from the MPU to the internal control registers and internal RAM of the XD1602A0 via an 8-bit bus interface or a serial interface. There are five types of internal control registers, as follows (details are described later):

- Index register: Selects and designates which control register the MPU is to access
- Status register: Indicates the internal state
- Control registers: Designates display control
- RAM address register: Sets an address for accessing the various RAMs
- RAM data register: Receives and transmits data to and from the various RAMs

Table 17 shows the instruction list and the number of execution cycles of each instruction after performing register setting. Instructions that perform data transfer with the RAM data register tend to be used the most. However, auto-incrementation by 1 (or auto decrementation by 1) of internal XD1602A0 RAM addresses after each data write can lighten the program load on the MPU. Note that when an instruction is being executed (internal operations are being performed), only the busy flag in the status register can be read.

Since the busy flag is 1 during execution, the MPU should check this value before accessing a register. When accessing a register without checking the busy flag, an interval longer than the instruction execution time is needed before the next access. Refer to Table 17 Instruction Registers, for instruction execution times.

When rewriting DDRAM, character display will momentarily breakdown if the data (character codes) that is being rewritten is also being read by the system for display. For this reason, check the display read line position (NF) and the display read raster-row position (LF) in the status register (SR), and rewrite a DDRAM line that is not being read and displayed.

Functional Description

Index Register (IR)

The index register (Figure 4) designates control registers (R0 to R7), RAM address register (RAR: R8), and RAM data register (RDR: R9). The register number must be set between addresses 0000 to 1001 in binary digits. Note that if address 1111 is set, the test register will be selected. Addresses 1010 to 1110 are ignored.

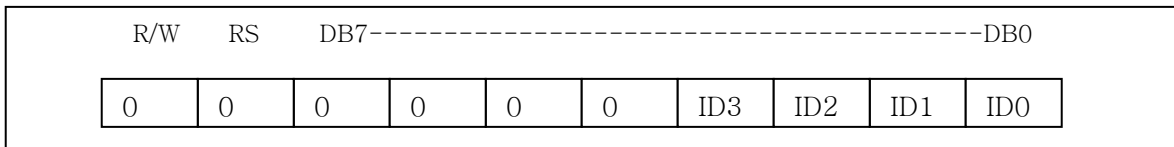


Figure 4 Index Register

Status Register (ST)

The status register (Figure 5) includes the busy flag (BF), display line bits (NF1/0), and display raster-row bits (LF0 to LF3). If BF is 1, an instruction is being executed, and another instruction will not be accepted during this time. Any attempt to write data to a register at this time is ignored.

Rasters-rows are driven one at a time according to specific timing to perform liquid crystal display. Bits NF1 and NF0 indicate display lines, and bits LF3 to LF0 indicate the raster-row in a line. If character display degenerates when rewriting DDRAM, rewrite only those display lines that are not currently being read out by the system for display. During segment display, the next state of the last raster-row in the character display is read out.

Table 9 Display State According to NF1 and NF0

NF1	NF0	Display State
0	0	Displaying the first line
	1	Displaying the second line
0		
1	0	Displaying the third line
1	1	Displaying the fourth line

Table 10 Display State According to LF3 to LF0

LF3	LF2	LF1	LF0	Display State
0	0	0	0	Displaying the first raster-row
0	0	0	1	Displaying the second raster-row
0	0	1	0	Displaying the third raster-row
0	0	1	1	Displaying the fourth raster-row
⋮				⋮
1	1	0	0	Displaying the 13th raster-row

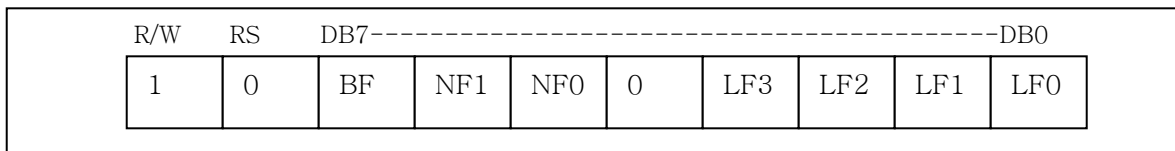


Figure 5 Status Register

Entry Mode Register (R0)

The entry mode register (Figure 6) includes bits I/D, RM1, and RM0.

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DDRAM address by 1 when a character code is written into or read out from the DDRAM. When the DDRAM address is incremented by 1, the cursor or blinking will also shift to the right. This applies to both CGRAM and SEGRAM.

RM1/0: Selects DDRAM, CGRAM, or SEGRAM for access (Table 10).

Table 11 RAM Selection by RM1 and RM0

RM1	RM0	Selected RAM
0	0/1	Display data RAM (DDRAM)
1	0	Character generator RAM (CGRAM)
1	1	Segment RAM (SEGRAM)

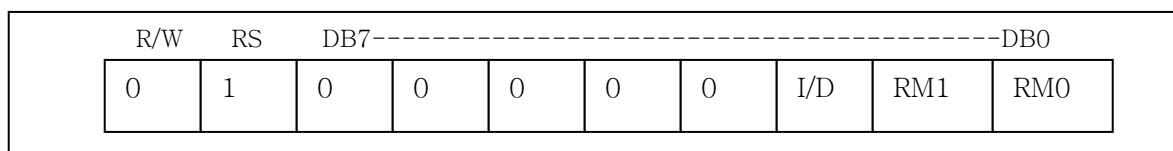


Figure 6 Entry Mode Register

Function Set Register (R1)

The function set register (Figure 7) includes bits BST, EXT2, EXT1, DT1, DT0, and DCL.

BST: When BST is 1, the booster starts to operate. When the LCD voltage is external, set BST to 0 to stop operation of the internal booster. In addition, the consumption current can be suppressed by stopping the booster when entering standby mode without display.

EXT2/1: Extends the common driver and segment driver of XD1602A0. Set EXT2 to 1 to extend the driver to the common side if the duty ratio is 1/40 or 1/53. Extend the driver to the segment side by setting EXT1 to 1 when displaying 7 or more digits (of full size) in the horizontal direction. DDRAM capacity is 80 bytes. When the XD1602A1, these EXT2/1 bits must be set to 1.

DT1/0: Selects the duty ratio of the LCD (Table 11). Although this bit can be set separately from the display line designation (NL1/0), the duty ratio must be selected so that it will be smaller than the number of display lines.

DCL: When DCL is 1, the display is cleared by writing the code for half-size space (H'A0) into all DDRAM addresses. Then H'00 is written into the RAM address counter (RAR) and the DDRAM is selected. The character code for character code H'A0 must be a blank pattern when rewriting HCGROM used for half-size characters.

Cursor Control Register (R2)

The cursor control register includes bits CHM, C, CM1, and CM0.

CHM: When CHM is set to 1, DDRAM is selected, the RAM address counter (RAR) is set to 0, and the cursor home instruction is executed. The contents of DDRAM do not change. The cursor or blinking moves to the left edge of the display (the left edge of the first line if two lines are displayed).

C: When C = 1, cursor display is turned on. The cursor is displayed at the position corresponding to the count value of the RAM address counter (RAR). To set data in the RAR, set the index register (IDR) to 1000 to select it, and modify the data in the RAR. Note that the RAM address counter (RAR) automatically increments (decrements) when the RAM is accessed, and the cursor will move accordingly.

CM1/0: Selects cursor display mode (Table 12 and Figure 9). The blinking frequency (cycle) of the blink cursor and the white/black inverted cursor has 64 frames.

Table 12 Duty Drive Ratio

DT1	DT0	Duty Drive Ratio
0	0	1/14 duty drive
0	1	1/27 duty drive

Table 13 Cursor Mode Selection

CM1	CM0	Selected Cursor Mode
0	0	12th raster-row cursor
0	1	Blink cursor
1	0/1	White/black inverted cursor

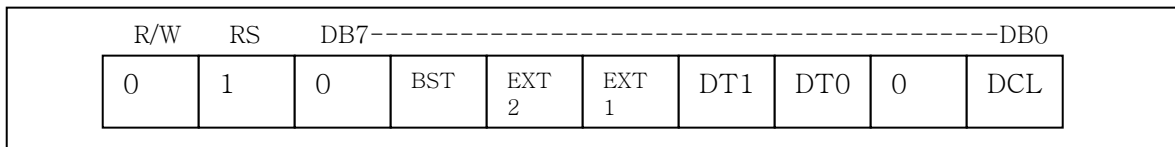


Figure 7 Function Set Register

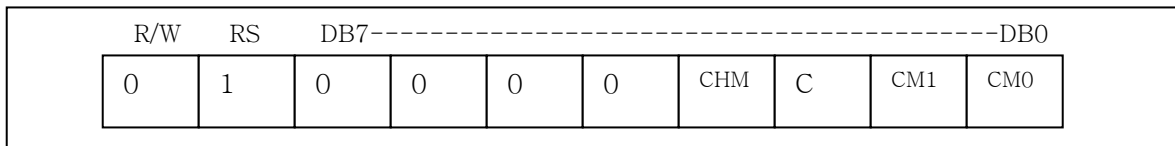


Figure 8 Cursor Control Register

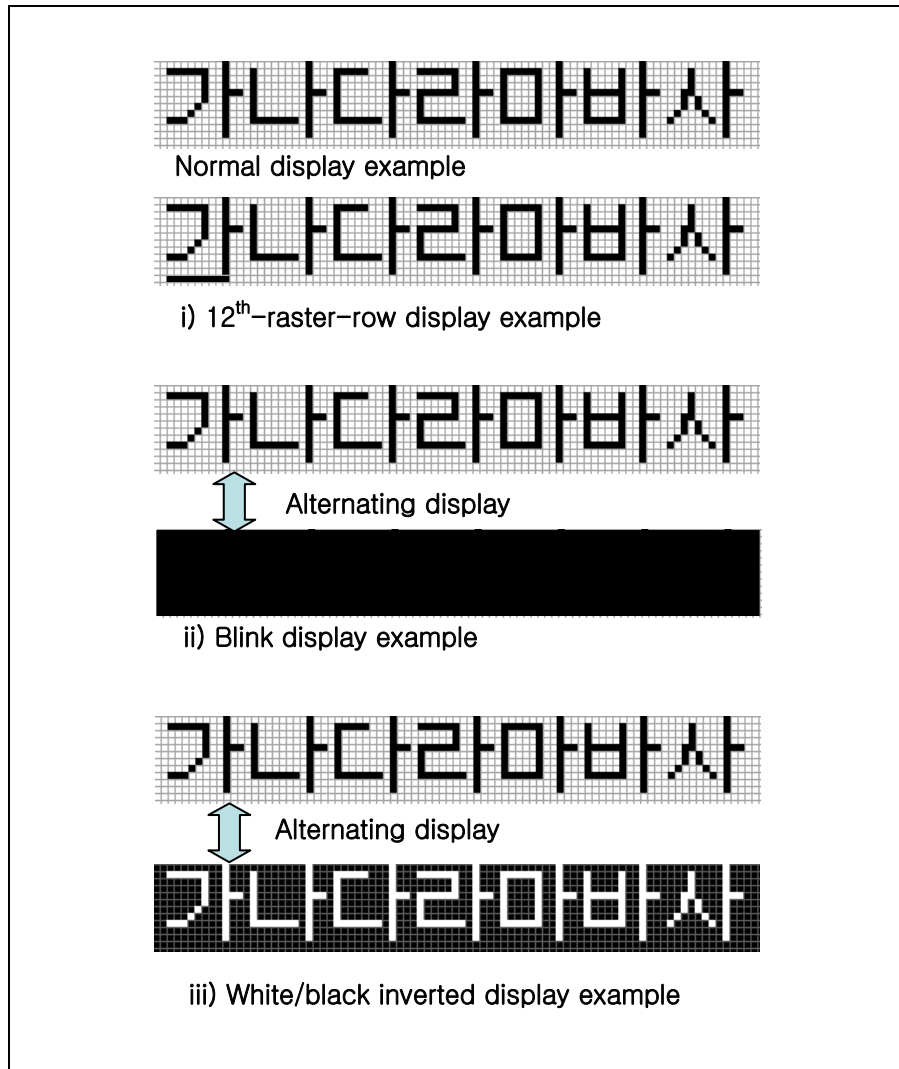


Figure 9 Cursor Display Examples

Display Control Register 1 (R3)

The display control register 1 (Figure 10) includes bits ST, DC, and DS.

ST: When ST is 1, the display control register 1 enters the standby mode. The internal operation clock is divided into 32. Data cannot be displayed on the LCD panel, however, the consumption current can be suppressed during the standby mode. Note that the register setting value and the data inside the RAM are maintained.

DC: When DC is 1, the character display is turned on.

DS: When DS is 1, the segment display is turned on. Bit DS can selectively display marks.

Display Control Register 2 (R4)

NC1/0: Selects the display character in the horizontal direction. When performing a horizontal smooth scroll, set the number of display characters larger than the actual number of liquid crystal drive characters. When the frame frequency (cycle) is stable, the operation frequency is proportional to the display characters. Operation frequency must be suppressed by setting the number of display character as small as possible because the consumption current is proportional to the operation frequency. Refer to Oscillator for details.

NL1/0: Sets the number of display lines. Set the number of display lines larger than the duty drive ratio (DT1/0). Do not set 10 to these bits. Table 13 indicates the settings of the display lines.

Table 14 Display Control Register 2 Setting

Display NL1/0	Lines Display Characters: NC1/0		
	00	01	10
00	1-line 6 characters	1-line 20 characters	1-line 40 characters
01	2-line 6 characters	2-line 10 characters	2-line 20 characters
10	Setting is inhibited		

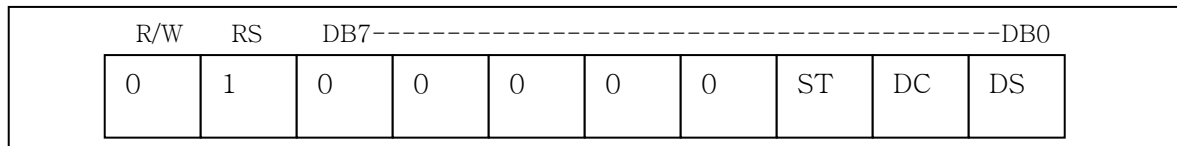


Figure 10 Display Control Register 1

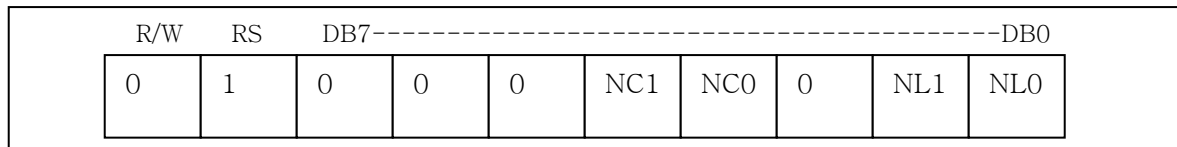


Figure 11 Display Control ReScroll Control Register 1 (R5)

The scroll control register 1 (Figure 12) includes bits SN1, SN0, SL3, SL2, SL1, and SL0.

SN1/0: Selects the starting line to be displayed. When SN1/0 shows 00, display begins from the first line. When SN1/0 shows 01, 10, 11, display begins from the second, third, or fourth line, respectively. Use these bits within the display line setting (NL1/0). SN can be used to display a smooth scroll and DDRAM memory bank switching.

SL0 to SL3: Selects the scroll starting raster-row of the line set by the start display line (SL1/0). When these bits show 0000, a display line starting from the head raster-row (first raster-row) is displayed and can be set to 1100 (13th raster-row) showing the last raster-row. A vertical smooth scroll can be performed by sequentially incrementing the first raster-row. Refer to Vertical Smooth Scroll for details. Note that bits SL0 to SL3 that are set to a value above 1100 will not operate correctly.

Scroll Control Register 2 (R6)

The scroll control register 2 (Figure 13) includes bits PS1, PS0, SE4, SE3, SE2, and SE1.

PS1/0: Selects the partial smooth scroll mode. When PS1/0 bits are 00, all characters scroll horizontally across the display. When bits PS1/0 are 01, only the leftmost character is fixed and the remaining characters perform horizontal smooth scroll display. When bits PS1/0 are 10, the two leftmost bits, and when 11, the three leftmost characters are fixed and the remaining characters perform horizontal smooth scroll. Refer to Partial Smooth Scroll for details.

SE1 to SE4: These bits enable a dot scroll in display lines designated by scroll control register 3 (R7). When bit SE is 1, the first line is scrolled according to scroll control register 3 (R7). When SE2 is 1, the second line scrolls independently, when SE3 is 1, the third line scrolls independently, when SE4 is 1, the fourth line scrolls independently. Scrolling multiple lines at the same time is also possible.

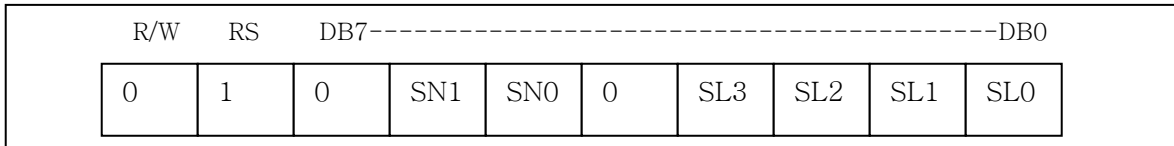


Figure 12 Scroll Control Register 1

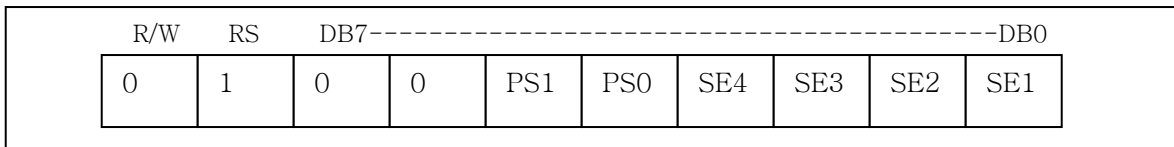


Figure 13 Scroll Control Register 2

Scroll Control Register 3 (R7)

The scroll control register 3 (Figure 14) includes bits SQ5, SQ4, SQ3, SQ2, SQ1, and SQ0.

SQ0 to SQ5: These bits designate the number of dots to be horizontally scrolled to the left on the panel. Horizontal smooth scroll can be performed for any number of dots between 1 and 48 inclusive by using the non-display DDRAM area. When these bits are 000000, scrolling is not performed. When these bits are 110000, 48 dots are scrolled to the left. If these bits are set to a value above 110000, 48 dots are still scrolled. Refer to Horizontal Smooth Scroll for details.

RAM Address Register (R8)

The RAM address register (Figure15) initially contains the RAM address at which incrementation (decrementation) starts. RAM selection bits (RM1/0) in the entry mode register (R0) select which RAM to access (DDRAM/CGRAM/SEGRAM). When DDRAM (RM1/0 = 00) is selected, address allocation differs according to the number of display lines, but in all cases the most significant bit (RA7) is ignored. During a 1-line display (NL1/0 = 00), addresses H'00 to H'4F are allocated to that line. During a 2-line display, addresses H'00 to H'27 are allocated to the first line, and addresses H'40 to H'67 are allocated to the second line. During a 4-line display, addresses H'00 to H'13 are allocated to the first line, H'20 to H'33 to the second, H'40 to H'53 to the third, and H'60 to H'73 to the fourth. See Table 14.

When CGRAM (RM1/0 = 10) is selected, addresses H'00 to H'19 are allocated to the first character and addresses H'20 to H'39 are allocated to the second character, and so on (Table 15). The setting of addresses between characters (example: H'1A to H'1F) is ignored here. When SEGRAM is selected (RM1/0 = 11), addresses H'0 to H'F are allocated to the RAM and the upper four bits (R4 to R7) are ignored (Table 16).

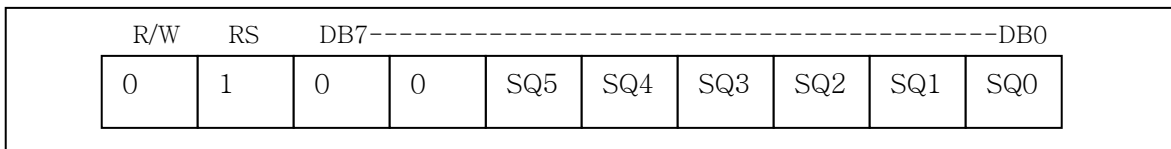


Figure 14 Scroll Control Register 3

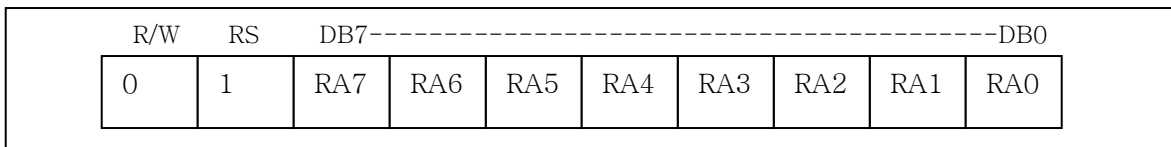


Figure 15 RAM Address Register

Table 15 DDRAM Address Allocation

Displayed Lines	1-Line Display	2-Line Display
	(NL1/0 = 00)	(NL1/0 = 01)
First line	H'00 to H'4F	H'00 to H'27
Second line	—	H'40 to H'67
Third line	—	—
Fourth line	—	—

Table 16 CGRAM Address Allocation

Displayed Character	CGRAM Address
First character	H'00 to H'19
Second character	H'20 to H'39
Third character	H'40 to H'59
Fourth character	H'60 to H'79
Fifth character	H'80 to H'99
Sixth character	H'A0 to H'B9
Seventh character	H'C0 to H'D9
Eighth character	H'E0 to H'F9

Table 17 SEGRAM Address Allocation

Displayed Segment SEGRAM Address	SEGRAM Address
SEG1 to SEG6	H'00
SEG7 to SEG12	H'01
SEG13 to SEG18	H'02
SEG19 to SEG24	H'03
SEG25 to SEG30	H'04
SEG31 to SEG36	H'05
SEG37 to SEG42	H'06
SEG43 to SEG48	H'07
SEG49 to SEG54	H'08
SEG55 to SEG60	H'09
SEG61 to SEG66	H'0A
SEG67 to SEG72	H'0B
SEG73 to SEG78	H'0C
SEG79 to SEG84	H'0D
SEG85 to SEG90	H'0E
SEG91 to SEG96	H'0F
SEG97 to SEG102	H'10
SEG103 to SEG108	H'11
SEG109 to SEG114	H'12
SEG115 to SEG120	H'13
SEG121 to SEG126	H'14
SEG127 to SEG132	H'15
SEG133 to SEG 138	H'16
SEG139 to SEG144	H'17
SEG145 to SEG150	H'18
SEG151 to SEG156	H'19
SEG157 to SEG162	H'1A
SEG163 to SEG168	H'1B
SEG169 to SEG174	H'1C
SEG175 to SEG180	H'1D
SEG182 to SEG186	H'1E
SEG188 to SEG192	H'1F

RAM Data Register (R9)

This register (Figure 16) stores 8-bit data that is written to or read from the DDRAM, CGRAM, or SEGRAM at the address indicated by the RAM address counter (RAC). The RAM selection bit (RM1/0) selects the RAM (DDRAM, CGRAM, SEGRAM). After the said RAM is accessed, RAM address is automatically incremented (decremented) by 1 according to the I/D bit.

Note that RAM selection bits (RM1/0) and RAM address register (R8) must be set before reading. If not, the first data read is invalid. If read instructions continue to be executed, however, data will be read correctly from the second read.

Test Register (RF)

This is a test register (Figure 17) and must be set to H'00 at all times. This register is automatically cleared (H'00) by reset input; however, it must be cleared by software after power-on if the reset pin is not used.

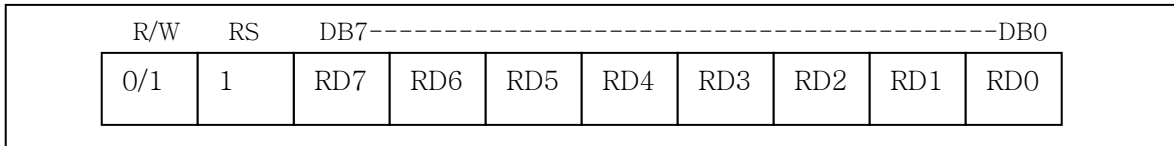


Figure 16 RAM Data Register

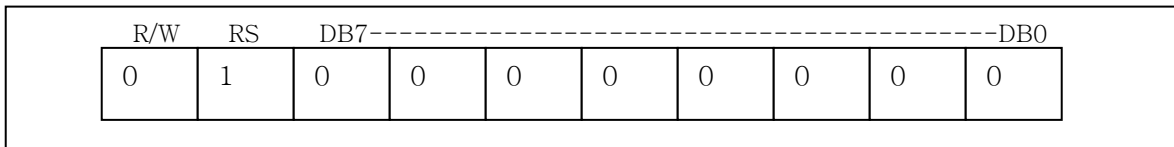


Figure 17 Test Register

Table 18 Instruction Registers

Reg No	Index (Hex)	Register	Code										Description	Execution Clock Cycle
			R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
IR	—	Index (IDR)	0	0	—	—	—	—	ID3	ID2	ID1	ID0	Designates the register number of the instruction register to access. ID = 0000: R0 to 1001: R9	12
SR	—	Status (STR)	1	0	BF	NF1	NF0	-	LF3	LF2	LF1	LF0	Indicates the busy flag (BF), display read line position (NF1/0), display read rasterrow position(NL0 to NL3).	0
R0	0	Entry Mode (EMR)	0	1	0	0	0	0	0	I/D	RM1	RM0	Designates RAM address in crementation or decrementation (I/D) and RAM selection (RM1/0).	12
R1	1	Function Set (FSR)	0	1	0	BST X	EX2	EX1	DT10	DT01	0	DCL	DCL Clears display (DCL) and initializes the DDRAM address. Selects duty drive ratio(DT1/0), enables extension driver (EX2/1) and sets the booster operation on.	DCL = 1: 492 Other: 12
R2	2	Cursor Control (CCR)	0	1	0	0	0	0	CHM	C	CM1	CM0	Designates cursor-on (C) and cursor display mode(CM1/0). Executes cursor home (CHM) instruction.	12
R3	3	Display Control 1 (DCR1)	0	1	0	0	0	0	0	ST	DC	DS	Designates standby mode (ST), character display on (DC), and segment display on (DS).	12
R4	4	Display Control 2 (DCR2)	0	1	0	0	NC1	NC0	0	0	NL1	NL0	Sets the number of display characters(NC1/0) and display lines(NL1/0).	12
R5	5	Scroll Control 1 (SCR1)	0	1	0	SN1	SN0	0	SL3	SL2	SL1	SL0	Sets the display start line (SN1/0) and start raster-row (ST0 to ST3).	12
R6	6	Scroll Control 2 (SCR2)	0	1	0	0	PS1	PS0	SE4	SE3	SE2	SE1	Designates partial scroll columns (PS1/0) and scroll display line enable(SE1 to SE4).	12
R7	7	Scroll Control3 (SCR3)	0	1	0	0	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Sets the number of dots to be scrolled (SQR0 to SQR5).	12

Table 18 Instruction Registers (cont)

Reg No	Index (Hex)	Register	Code										Description	Execution Clock Cycle
			R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
R8	8	RAM Address (RAR)	0	1	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	Resets the address address counter for DDRAM/CGRAM/SEGRAM. RAM is selected by RM1/0.	12
R9	9	RAM Data (RDR)	0/1	1	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	Writes or reads data to and from DDRAM/CGRAM/SEGRAM. RAM is selected by RM1/0.	12
RF	F	Test (TSR)	0	1	0	0	0	0	0	0	0	0	This is a test register. Set 00 in this register.	12

Note: The execution time depends on the input or oscillation frequency.

BF = 1: Internal processing being performed

NF1/0: Position of display read line

LF0 to LF3: Position of display read raster-row

ID= 1: Address increment

= 0: Address decrement

RM1/0: RAM selection (00/01: DDRAM, 10: GGRAM, 11: SEGRAM)

BST = X: Always Booster on

EX2 = 1: Common driver extension enable

EX1 = 1: Segment driver extension enable

DT1/0: Duty ratio (01: 1/27)

DCL = 1: Executes display-clear instruction

CHM = 1: Executes cursor-home instruction

C = 1: Cursor on

CM1/0: Designates cursor mode (00: 12th raster-row, 01: blinking, 10: white/black inverse)

ST = 1: Standby mode

DC = 1: Character display on

DS = 1: Segment display on

NC1/0: Sets the number of display characters (6 to 40 characters)

NL1/0: Sets the number of display lines (00: 1 line, 01: 2 lines, 11: 4 lines)

SN1/0: Designates the line to start displaying (00: first line, 01: second line, 10: third line, 11: fourth line)

SL0 to SL3: Designates scroll starting raster-row(0000: first raster-row, 1100: 13th raster-row)

PS1/0: Designates partial scroll (00: all columns scroll. 01: the leftmost column fixed, 10: the two leftmost columns fixed, 11: the three leftmost columns fixed)

SE1 to SE4: Designates which line to scroll (SE = 1: enables the first line to be scrolled, etc.)

SQ0 to SQ5: Number of dots to scroll (0 to 48 dots)

RA0 to RA7: RAM address

RD0 to RD7: RAM data

Reset Function

The XD1602A0/1 is reset by setting the RESET pin to low level. During reset, the system performs next control-

register setting and executes instructions. The busy flag (BF) therefore indicates a busy state (BF = 1) at this time, which means that only the index register and status register can be accessed. Display clear (DDRAM reset) is performed automatically by reset input. Since more than 1,000 clocks of execution cycles are needed to initialize the DDRAM, the reset period must be set to more than this number. Note that if the reset input conditions specified in Electrical Characteristics are not satisfied, the XD1602A0/1 will not operate correctly, and reset should be performed by software.

Initialization of Instruction Register Function

1. Index Register: IR

The index register cannot be initialized by reset. After reset release, the index register must be set to access a control register.

2. Status register: SR

BF = 1: Busy state

3. Entry mode register: R0

I/D = 1: +1 (incrementation)

RM1/0 = 00: DDRAM selection

4. Function set register: R1

BST = X (Don't care): Always Booster on

EX2/1 = 11: Driver extension enable

DT1/0 = 10: 1/27 duty drive

DCL = 1: Display-clear execution

Note: At least 1,000 clock cycles of execution time is needed to clear the DDRAM.

5. Cursor control register: R2

CHM = 1: Cursor home execution

C = 0: Cursor display off

CM1/0 = 00: 12th raster-row cursor display mode

6. Display control register 1: R3

ST = 0: Standby mode clear

DC = 0: Character display off

DS = 0: Segment display off

7. Display control register 2: R4

NC1/0 = 00: 6-column display mode

NL1/0 = 00: 1-line display mode

8. Scroll control register 1: R5

SN1/0 = 00: Starts displaying from the first line.

SL3 to SL0 = 0000: Starts displaying from the first raster-row.

9. Scroll control register 2: R6

PS1/0 = 00: Partial scroll release

SE4 to SE1 = 0000: Disables dot scrolling for all lines.

10. Scroll control register 3: R7

SQ5 to SQ0 = 000000: Number of dots to be scrolled = 0

11. RAM address register: R8

RAM address register is automatically incremented during reset when display-clear is executed. Note that after reset is released, this register must be reset by software before accessing RAM.

Initial Setting of Pin Functions

1. Bus/serial interface

The input level of pin IM selects the 8-bit bus or serial interface. For an 8-bit bus interface, data is written into the index register or read from the status register according to the level of pin R/W. Note that pin RS must be held low during this time. For serial interface, data is written into the index register according to bit R/W. Note that bit RS must be 0 during this time. During reset, only the index register and status register can be set and RAM cannot be accessed.

2. LCD driver output

Since segment drivers (pins SEG1 to SEG191) are in a display-off state during reset, they output non-selective levels (V2/V3 level) during reset. At this time, a 2-line 16-character display alternates its current. Common drivers (pins COM1 to COM24) output non-selective levels (V1/V4 level) during reset, and alternate its current for a 2-line 16-character display.

3. Extension driver interface output (XD1602A0)

Since bits EX2/1 are 11 during reset, extension is performed to both segment side and common side. Pin CL2 outputs the oscillation (operation) frequency clock. Pins CL1 and M output signals in a cycle corresponding to a 2-line 16-character display size. In addition, pins SEGD and COM25 output low (ground level) since the display is turned off.

4. Booster output

The operation of the internal booster stops because bit BST becomes 0 during reset.

Note: The potential of pins V5OUT2 and V5OUT3 increases by about +0.7 V with respect to GND level when the booster stops. When using external polarized capacitors, make sure that no reverse bias occurs.

Interfacing to the MPU

The XD1602A0 enters 8-bit bus interface mode when the IM pin is set high. The XD1602A0 can interface with the MPU via an I/O port. Use the serial interface when there are restraints in the bus wiring width. Instruction is executed when data is written into the control register. In this case, only the status register can be read (busy check, etc.). In this case, check the busy flag when accessing (polling), or insert an interval considering the execution time and perform the next access when the internal process has completely finished. The instruction execution time depends on the XD1602A0 operation frequency. When using the internal oscillation circuit of the XD1602A0, the instruction time will change as the oscillation frequency does. Figure 18 shows an example of an 8-bit data transfer timing sequence. Figure 19 shows an example of interface between XD1602A0 and 8-bit microcomputers.

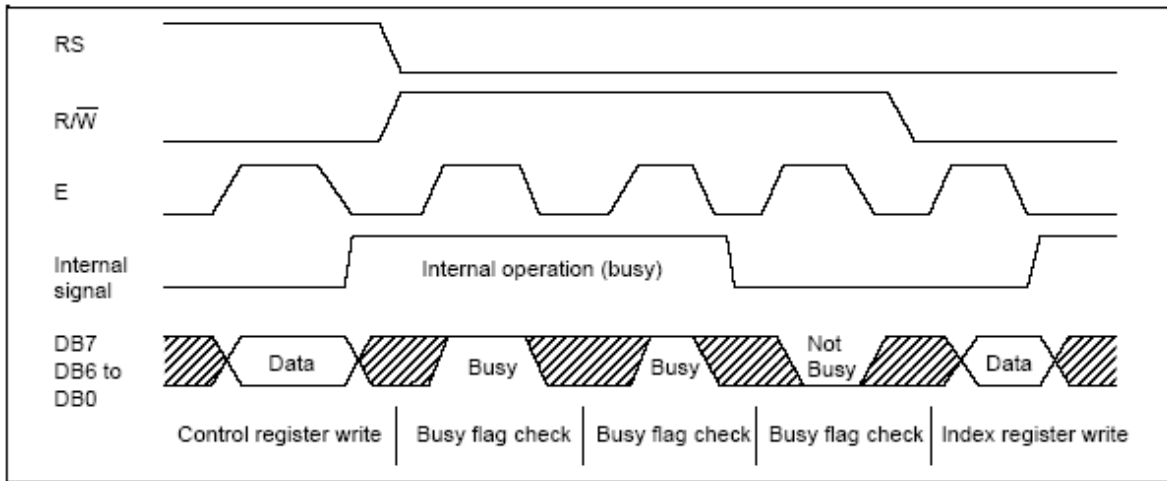


Figure 18 Example of an 8-bit Data Transfer Timing Sequence

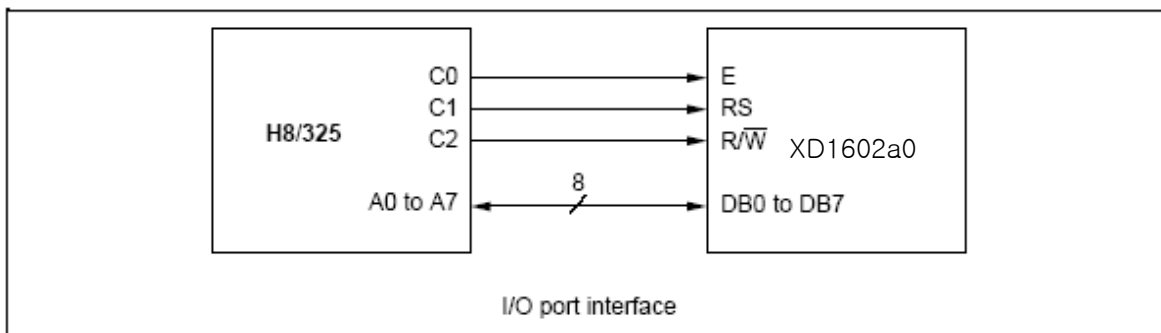


Figure 19 Example of Interfacing with 8-Bit Microcomputers

Combined Display of Full-Size and Half-Size Characters

The XD1602A0 performs display from the left edge of the display combining 12-dot full-size (character size: 11 × 12 dots) and 6-dot half-size characters (character size: 6 × 12 dots). There will be a one-dot space between these fonts.

The most significant bit in the data (8 bits) in DDRAM is allocated to the designation bit indicating a fullsize or half-size character. When this MSB is 0, the full-size character is selected, and when 1, the half-size character is selected.

When the full-size character is selected, 2 bytes of DDRAM are linked and used as a 16-bit code (Figure 22). In this case, the lower byte is written into the smaller DDRAM address. 12 bits of this 16-bit code are used as character codes. Up to 4096 character codes can be specified. In addition, two of the remaining four bits can be allocated to a display-attribute code and can designate white/black inverted display for individual characters (refer to Display Attribute Designation). The XD1602A0 12-bit character code. 8-bit data designating half-size characters are used as an 8-bit code (Figure 23). Specifically, 7 bits of the 8-bit half-size characters become the character codes, so that a total of 128 characters can be displayed (alphanumeric characters and symbols can be displayed as half-size characters).

User fonts can be displayed using the CGRAM. Special symbols not included in the internal CGROM or the KSC5601 Set can be displayed as needed. Since the display font size of the CGRAM is 12 × 13 dots, CGRAM fonts can be displayed to the right, left, top or bottom, in order to be used to display doublesize characters or graphics. Note that the display-attribute code (A1/A0) designation that is to be written into the DDRAM is ignored when the CGRAM is used. In this case, bits 6 and 7 in the CGRAM are used for display-attribute-code designation. Refer to CGRAM for details.

Table 19 Relationship between Korean Codes and XD1602A0 Character Codes

Korean	KSC5601 Code(16bit)	XD1602A0 Character Codes(12bit)
가	0x B0A1	0x400
각	0x B0A2	0x 401
간	0x B0A3	0x 402
갈	0x B0A4	0x 403
갸	0x B0A5	0x 404
갓	0x B0A6	0x 405

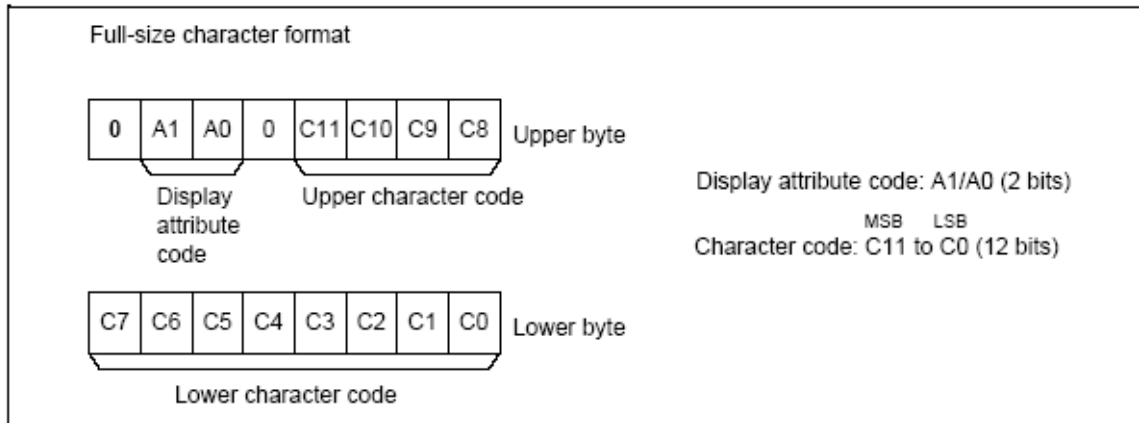


Figure 22 Full-Size Character Codes

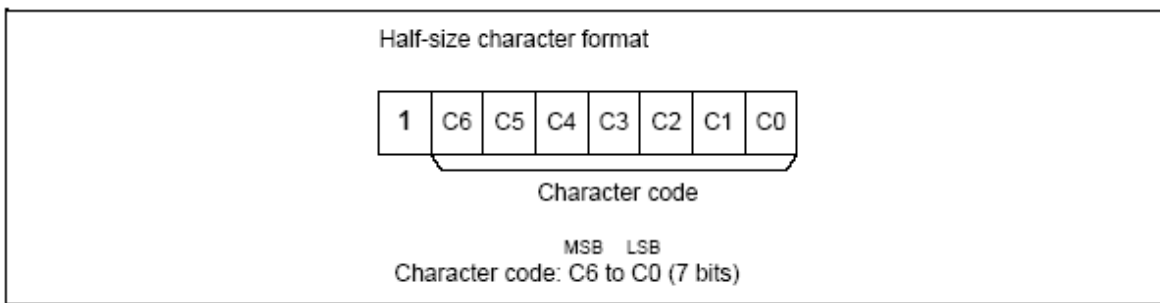


Figure 23 Half-Size Character Codes

An example of displaying full-size and half-size characters together is described here. Full-size character display conforms to KSC5601 (16 bits). Perform code conversion (16 bits → 12 bits) according to the relationship between the 16-bit Korean code and the XD1602A0 12-bit character code and write two-byte character data to the DDRAM (write the lower byte to the smaller DDRAM address). The example is shown in Table 19. When displaying a half-size character, refer to Page-22 the XD1602A0 Half-Font

Table 21 Example of Half-Size Font Code

Display Character	Character Code (C0 to C11)
1	31 (Hex)
2	32(Hex)
0	30(Hex)
.	2C(Hex)
M	4D(Hex)
C	43(Hex)

Display Attribute Designation

The XD1602A0 allocates 12 bits of the full-size 16-bit code character to an abbreviated character code and 2 bits to a display-attribute code (Figure 26). White/black inverted display, blinking display, and white/black inverted blinking display can be designated for each full-size character (Table 21). Display attribute control is performed for a 12 × 13 dot matrix unit that includes a 11 × 12 dot full-size character and a column of dots to the right and a row of dots to the bottom (Figure 27). The blinking cycle for blinking display and white/black inverted blinking display is 64 frames. Blinking display is performed by changing the display pattern every 32 frames. Since the 8-bit code designated for half-size characters cannot accommodate a display attribute, they will always be displayed normally.

Table 22 Display Attribute Designation

A1	A0	Display State
0	0	Normal display
0	1	White/black inverted display
1	0	Blinking display
1	1	White/black inverted blinking display

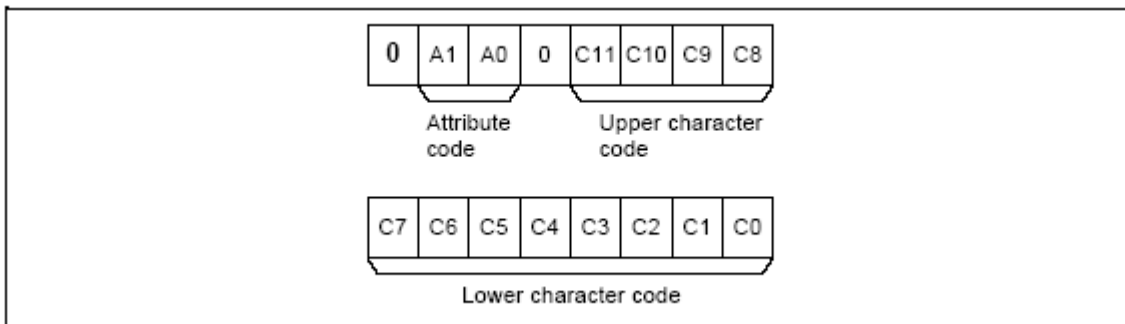


Figure 26 Full-Size Code Format



Figure 27 Setting Codes in the DDRAM and Display Examples

Horizontal Smooth Scroll

Data shown on the display can be scrolled horizontally to the left for a specified number of dots (Figure 28). The number of dots are set in scroll control register 3 (SCR3: R7), and the display lines to be scrolled are designated by the display line enable bits (SE1/SE2/SE3/SE4) in scroll control register 2 (SCR2: R6). Because the number of dots that can be set for scrolling here is 48, scrolling for more than this number can be achieved by shifting to the left by four characters of character code data in DDRAM for the scroll display line in question, rewriting the characters, and then scrolling again. When rewriting DDRAM while displaying characters, however, character output will momentarily breakdown, and the display may flicker. In this case, first check which display lines are currently being displayed by referring to NF1/0 (line 1 to the line 4) and display raster-rows LF0 to LF3 (raster-row 1 to raster-row 13) in the status register, and then rewrite a DDRAM line that is not being displayed. Keep in mind that scroll display line enable bits (SE1 to SE4) can be used to designate those display lines for which horizontal smooth scroll is desired. In partial scroll, one to three leftmost characters on the display as specified by the partial scroll bits (PS1/0) of the scroll control register 2 (SCR: R6) are fixed and the remaining characters undergo a smooth scroll to perform partial smooth scroll.

When performing horizontal smooth scroll, the number of characters to be displayed (NC1/0: R4) must be at least 4 characters more than the number of characters actually displayed on the liquid crystal display. For example, set 10 or more display characters (NC1/0) for a single-chip 6-character display.

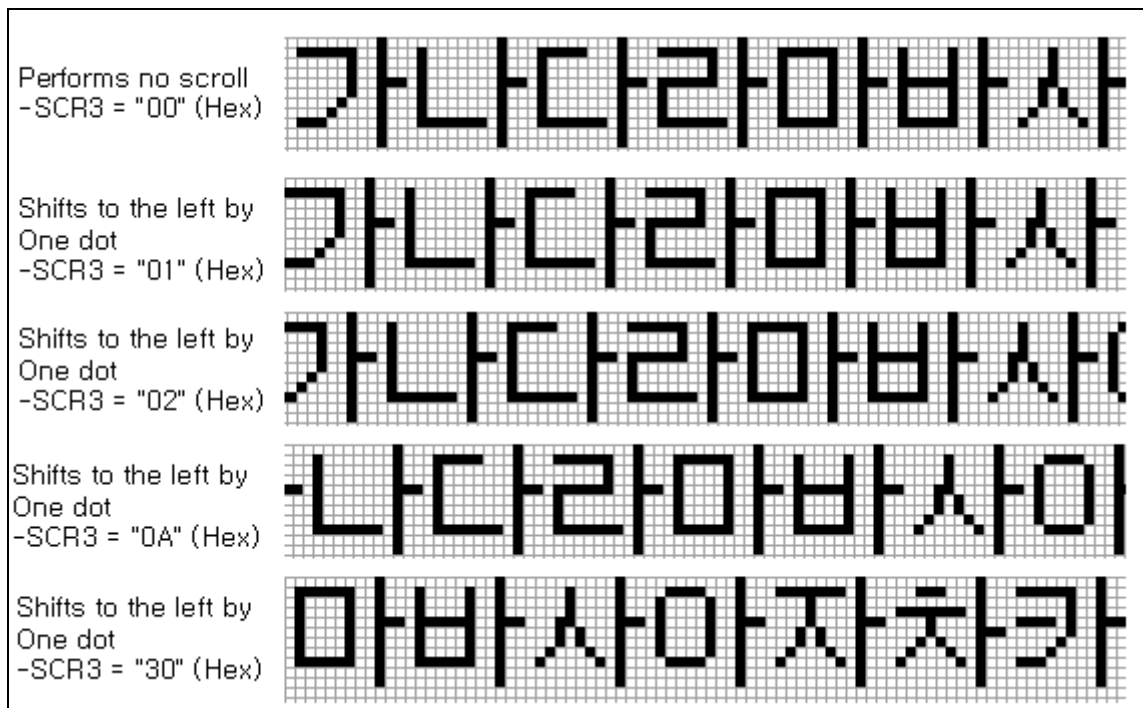


Figure 28 Example of Horizontal Smooth Scroll Display

Examples of Register Setting

	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	0	0	0	0	0	0	0	1	1	0	Index register set (R6 designation)
2	0	1	0	0	0	1	0	0	1	0	Enables scroll (scrolls only the second line)
3	0	0	0	0	0	0	0	1	1	1	Index register set (R7 designation)
4	0	1	0	0	0	0	0	0	0	1	Shifts the second line to the left by one dot
CPU Wait											
5	0	1	1	0	0	0	0	0	1	0	Shifts the second line to the left by two dots
CPU Wait											
6	0	1	1	0	0	0	0	0	1	1	Shifts the second line to the left by three dots
CPU Wait											
⋮											
51	0	1	1	0	1	1	0	0	0	0	Shifts the second line to the left by 48 dots*

Note: The number of dots that can be specified for scrolling is 48. Scrolling for more than this number can be achieved by rewriting DDRAM data and scrolling again from dot 0.

Note that the number of characters shown on the LCD and the number of scroll characters must be less than the number of maximum display characters (1-line display mode:

40 characters, 2-line display mode: 20 characters).

Figure 29 Example of Executing Smooth Scroll to the Left

	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	0	0	0	0	0	0	0	1	1	0	Index register set (R6 designation)
2	0	1	0	0	0	1	0	0	1	0	Enables scroll (scrolls only the second line)
3	0	0	0	0	0	0	0	1	1	1	Index register set (R7 designation)
4	0	1	1	0	1	1	0	0	0	0	Shifts the second line to the left by 48 dots*
CPU Wait											
5	0	1	1	0	1	0	1	1	1	1	Shifts the second line to the left by 47 dots
CPU Wait											
⋮											
49	0	1	1	1	0	0	0	0	0	1	Shifts the second line to the left by one dot
CPU Wait											
51	0	1	1	0	0	0	0	0	0	0	Perform no shift

Note: The number of dots that can be specified for scrolling is 48. Rewrite 48 dots (4 characters) of data inside the DDRAM and shift them to the right before scrolling. Scrolling for more than this number can be achieved by rewriting the data of DDRAM and begin scrolling from dot 48 again. Note that the number of characters shown on the LCD and the number of scroll characters must be less than the number of maximum display characters (1-line display mode: 40 characters, 2-line display mode: 20 characters).

Figure 30 Example of Executing Smooth Scroll to the Right

Partial Smooth Scroll

Partial smooth scroll displays one to three leftmost characters as fixed while the remaining ones undergo a horizontal smooth scroll in the left and right direction. Specifically, the number of leftmost characters to be fixed is specified by the partial scroll bits (PS1/0) in the scroll control register 2 (SCR2: R6). For example, when bits PS1/0 are 10, the two leftmost characters are fixed; when 11, the three leftmost characters are fixed.

Although half-size characters can be displayed in a fixed display area, they must be displayed in even-numbered groups of two, four or six characters. Figure 31 shows an example of smooth scroll performed in a display when bits PS1/0 are set to 10. The two leftmost characters (가나) are displayed as fixed, and the remaining four characters undergo a smooth scroll.



Figure 31 Example of Partial Smooth Scroll Display

Vertical Smooth Scroll

Vertical smooth scroll up and down can be performed by setting the number of display lines (NL1/0: R4) to a value greater than the actual number of liquid crystal display lines, which can be set by the duty drive ratio (DT1/0: R1) to 1/14 (1-line display), 1/27 (2-line display). The display line setting (NL1/0: R4), which controls the display, can select 1-line display mode, 2-line display mode.

For example, to perform normal vertical smooth scroll for a 2-line liquid crystal display with a duty ratio of 1/27, set the number of display lines (NL1/0: R4) to 2 lines.

Note that if vertical smooth scroll is performed when the number of actual liquid display lines is the same as the number of set display lines, the display line that has scrolled out of the display will appear again from the bottom (or the top) (this function is called lap-around).

Vertical smooth scroll is controlled by incrementing or decrementing the display line (SN1/0), which indicates which line to start from, and the display raster-row (SL0 to SL3). For example, when performing smooth scroll up, the display raster-row (SL0 to SL3) is incremented from 0000 to 1100 in order to scroll 12 raster-rows. Moreover, by incrementing the display line (SN1/0) and then incrementing the display raster-row from 0000 to 1100 again, a total of 25 raster-rows can be scrolled. Since the DDRAM is only 80 bytes, its data must be rewritten when performing continuous scroll exceeding this capacity.

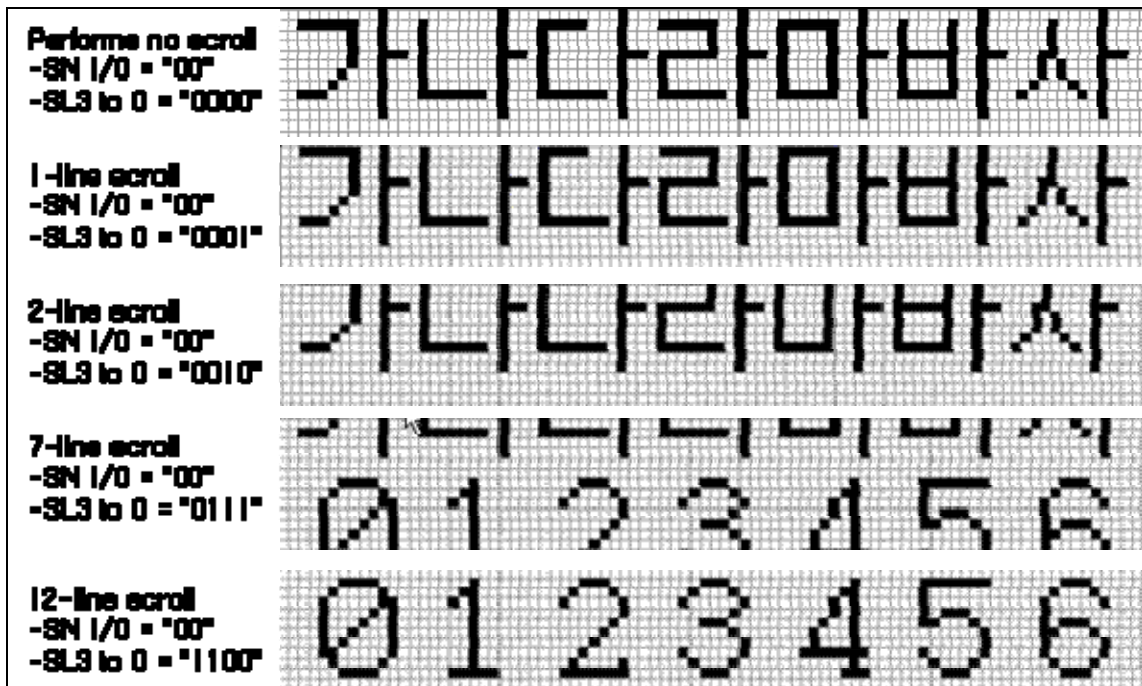


Figure 32 Example of Vertical Smooth Scroll Display

Examples of Register Setting (2-Line Liquid Crystal Drive: DT1/0 = 01, 2-Line Display Mode: NL1/0 = 10)

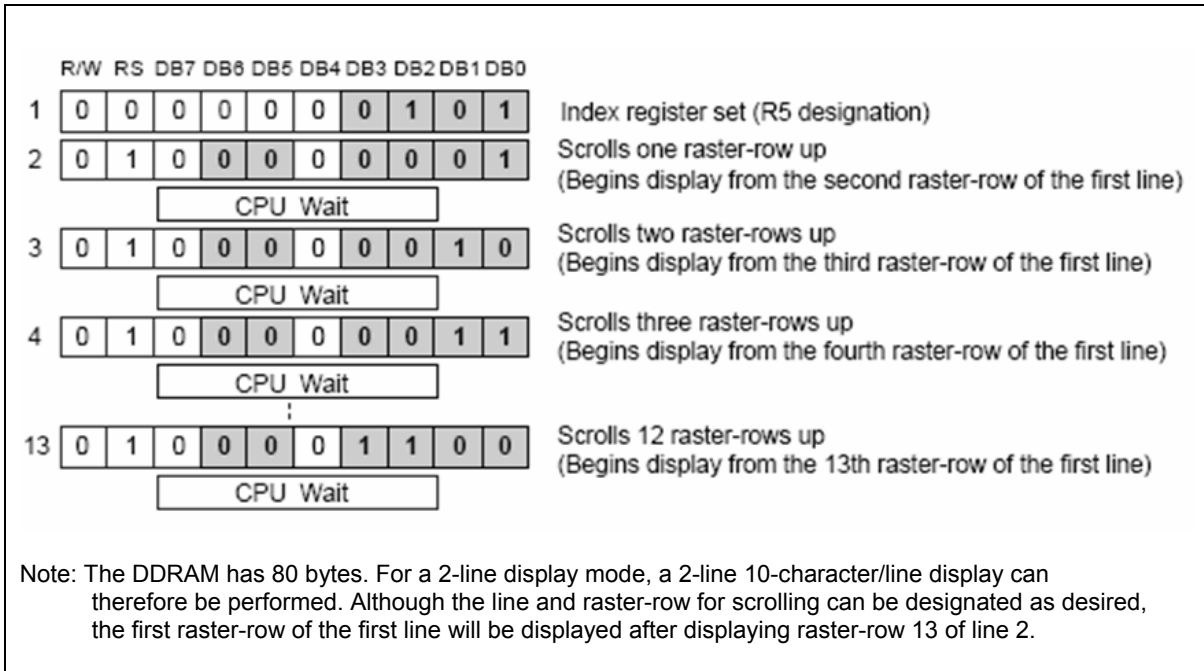


Figure 33 Example of Performing Smooth Scroll Up

Interfacing with the Liquid Crystal Panel

By connecting the XD1602A0 to extension drivers, the display can be 1-line/40-character, 2-line/20-character display configuration. Bits DT1/0 set the duty drive ratio and bits NC1/0 set the number of characters per line. In addition, bits NL1/0 sets the number of display lines during display read control. Table 22 shows the relationship between the number of characters actually displayed on the liquid crystal panel and the corresponding number of extension drivers needed.

Table 23 Relationship between the Number of Liquid Crystal Display Characters and Extension

Display Lines	Number of Display Characters per Line						Duty Drive
	6 Characters	10 Characters	12 Characters	16 Characters	20 Characters	40 Characters	
1 line	(0/0)	(2/0)	(2/0)	(3/0)	(5/0)	(11/0)	1/14
2 line	(0/0)	(2/0)	(2/0)	(3/0)	(5/0)	Display disabled	1/27

- Notes:
1. Numbers in parentheses = (number of extension segment drivers/number of common drivers)
 2. This is an example when using the 40 output extension drivers, and when N_h represents display characters and N_d extension driver outputs, the number of extension drivers needed can generally be calculated as follows:

$$[\text{Number of extension drivers}] = (12 * N_h - 71 - 1) / N_d \uparrow$$
 3. The right-edge segment (space between characters) is not displayed 16-character display.
 4. Horizontal smooth scroll cannot be performed during an 1-line/40-character, 2-line/20-character display.

Interfacing between XD1602A0

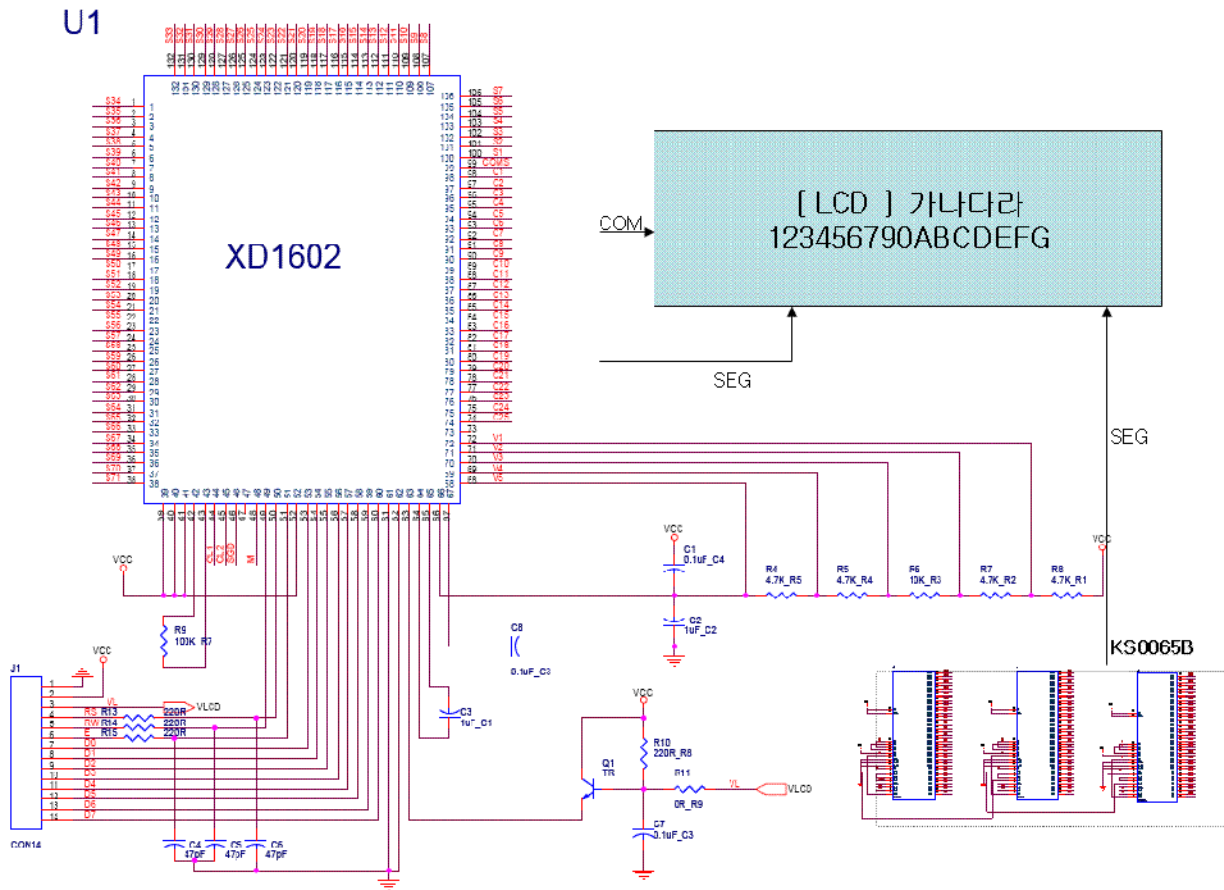


Figure 40 Example of Display Circuit

Oscillator

Figure 41 shows the optimal value of the oscillation frequency or the external clock frequency depends on the duty drive ratio setting (DT1/0), number of display lines (NL1/0), and the number of display characters (NC1/0) in the XD1602A0. The oscillation frequency or the external clock frequency must be adjusted according to the frame frequency of the liquid crystal drive.

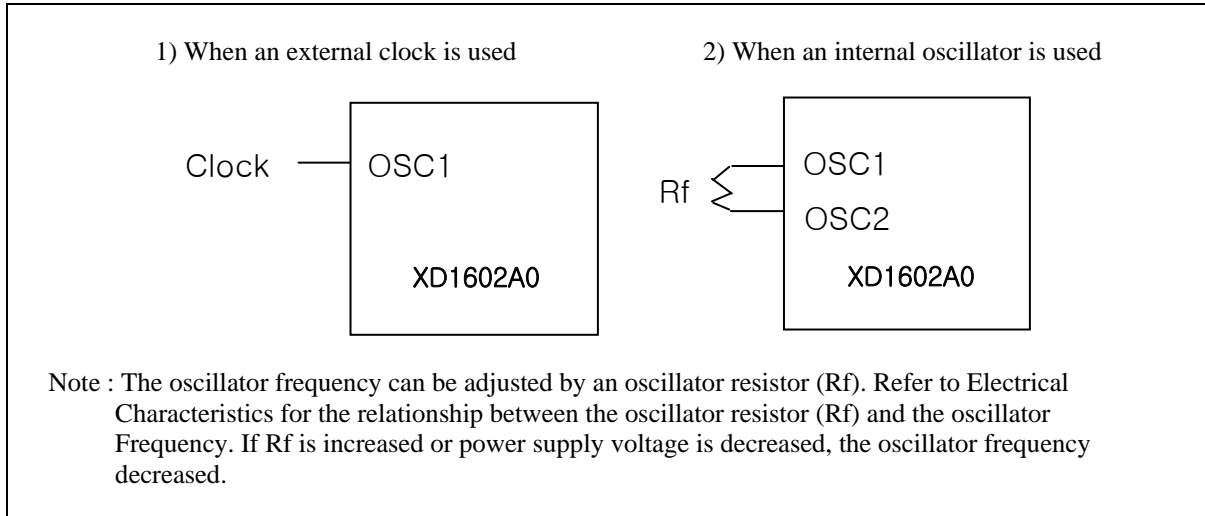


Figure 41 Oscillator Connections

Relationship between the Oscillation Frequency and the Liquid Crystal Display Frame Frequency

Number of Display Lines: (NL1/0 Set Value):	1-Line Display (00)		
	Number of display characters	6 characters	20 characters
(NC1/0 set value)	(00)	(01)	(11)
1-line selection period (dot)	72 dots	120 dots	240 dots
Number of dots per screen (dot)	1008 dots	1680 dots	3360 dots
Oscillation frequency (kHz)*	70	120	235

Notes: * The frequencies in Table 23 are examples when the frame frequency is set to 70 Hz. Adjust the oscillation frequency so that a optimum frame frequency can be obtained.

1/27 Duty Cycle (DT1/0 = 01: 2-Line Drive)

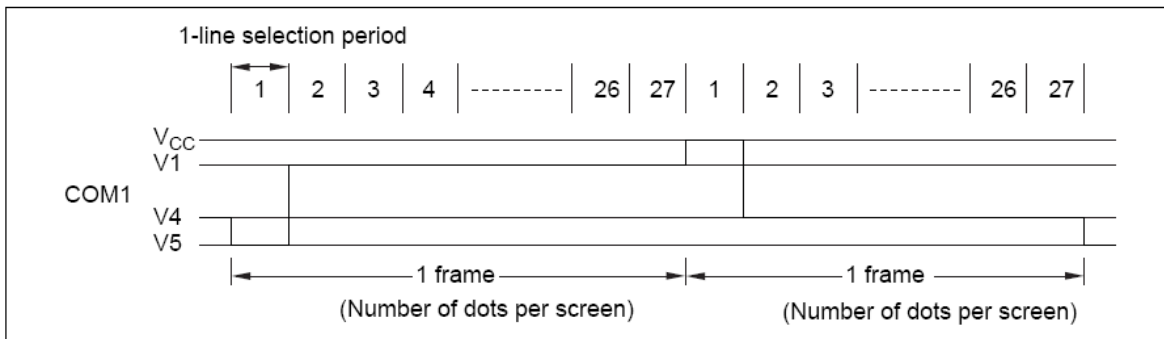


Figure 43 Frame Frequency (1/27 Duty Cycle)

Table 25 1/27 Duty Drive

Number of Display Lines: (NL1/0 Set Value):	1-Line Display (00)		
	Number of display characters	6 characters	10 characters
(NC1/0 set value)	(00)	(01)	(11)
1-line selection period (dot)	72 dots	120 dots	240 dots
Number of dots per screen (dot)	1944 dots	3240 dots	6480 dots
Oscillation frequency (kHz)*	135	225	475

Notes: * The frequencies in Table 24 are examples when the frame frequency is set to 70 Hz. Adjust the oscillation frequency so that an optimum frame frequency can be obtained.

Power Supply for Liquid Crystal Display Drive

The XD1602A0/1 incorporates a booster for raising the LCD voltage two or three times that of the reference voltage input below V_{CC} (Figure 48). A two or three times boosted voltage can be obtained by externally attaching two or three 1- μ F capacitors.

If the LCD panel is large and needs a large amount of drive current, the values of bleeder resistors that generate the V1 to V5 potential are made smaller. However, the load current in the booster and the voltage drop increases in this case.

We recommend setting the resistance value of each bleeder larger than 4.7 k Ω and to hold down the DC load current to 0.4 mA if using a booster circuit. An external power supply should supply LCD voltage if the DC load current exceeds 0.7 mA (Figure 49). Refer to Electrical Characteristics showing the relationship between the load current and booster voltage output. Table 27 shows the duty factor and bleeder resistor value for power supply for liquid crystal display drive.

Table 28 Duty Factor and Bleeder Resistor Value for Power Supply for Liquid Crystal Display Drive

Item		Data	
Drive lines (DT1/0 setting value)		1	2
Duty factor 1/14 1/27		1/14	1/27
Bias		1/4.7	1/6.2
Bleeder resistance value	R1	R	R
	R0	R*0.7	R*2.2

Notes: * R changes depending on the size of a liquid crystal panel. Normally, R must be 4.7 k Ω to 20 k Ω . Adjust R to the optimum value with the consumption current and display picture quality.

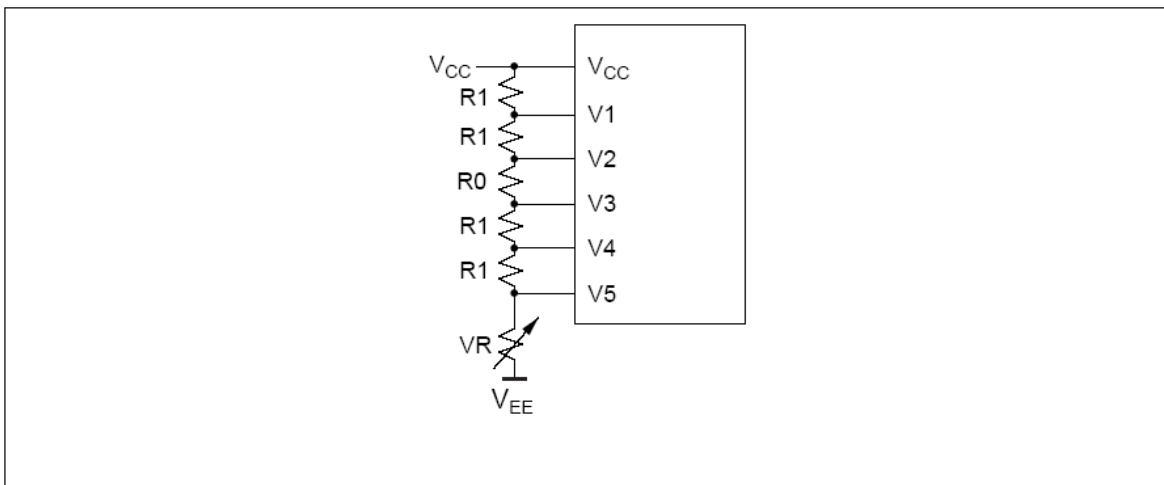


Figure 46 Example of Power Supply for Liquid Crystal Display Drive (with External Power Supply)

The reference voltage input (Vci) must be set below the power supply (Vcc). Current that flows into reference voltage input (Vci) is 2-3 times larger than the load current flowing through bleeder resistors. Note that a reference voltage drop occurs due to the current flowing into the Vci input when a reference voltage (Vci) is generated by resistor division.

The amount of output voltage (V5OUT2/V5OUT3) drop of a booster circuit also increases as the load current flowing through bleeder resistors increases. Thus, set the bleeder resistance as large as possible (4.7 kΩ or greater) without affecting display picture quality.

Adjust the reference voltage input (Vci) according to the fluctuation of booster characteristics because the output voltage (V5OUT2/V5OUT3) drop depends on the load current, operation temperature, operation frequency, capacitance of external capacitors, and manufacturing tolerance. Refer to Electrical Characteristics for details.

Adjust the reference voltage input (Vci) so that the output voltage (V5OUT2/V5OUT3) after boosting will not exceed the absolute maximum rating of liquid crystal power supply voltage (15V). Make sure that you connect polarized capacitors correctly.

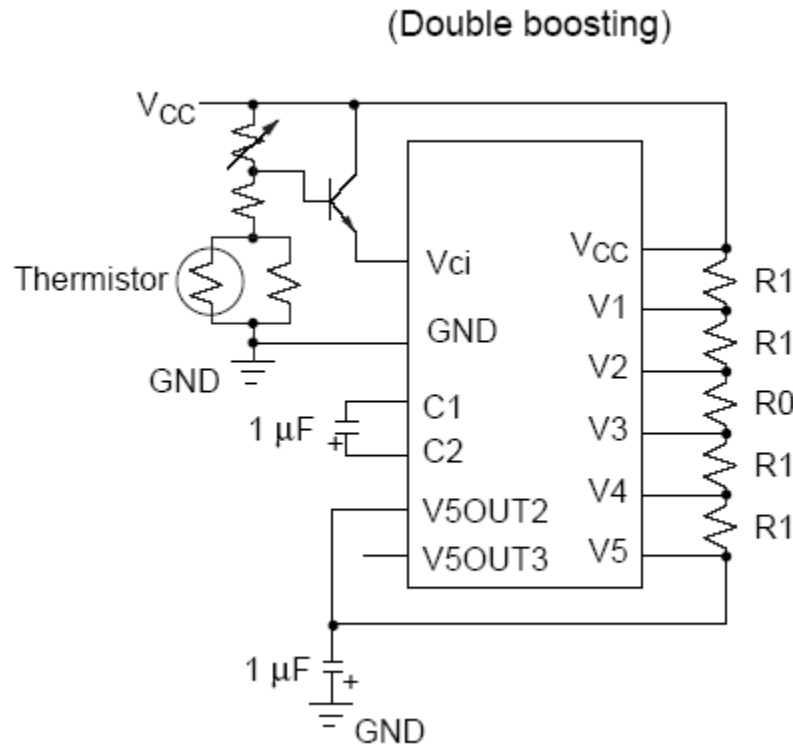


Figure 47 Example of Power Supply for Liquid Crystal Display Drive (with Internal Booster)

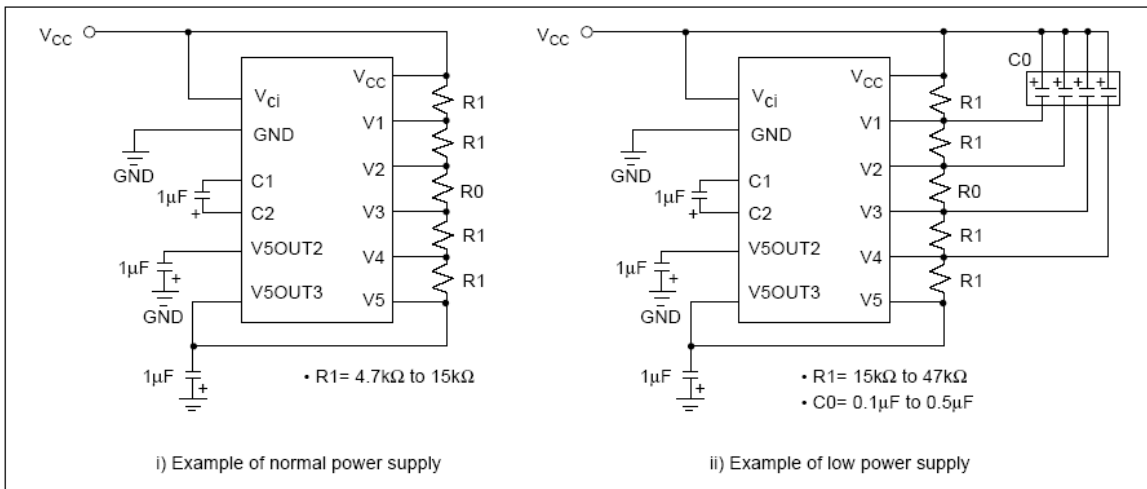


Figure 48 Example of Power Supply for Low Power Consumption

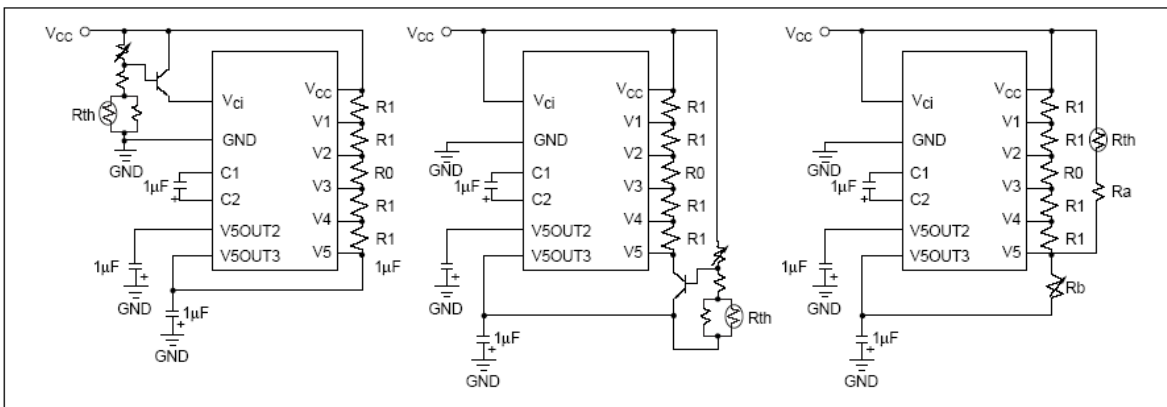


Figure 49 Example of Temperature Compensation Circuit

Absolute Maximum Ratings (XD1602A0)*

Item	Symbol	Value	Unit	Notes
Power supply voltage (1)	V_{CC}	-0.3 to +7.0	V	1
Power supply voltage (2)	$V_{CC}-V_5$	-0.3 to +17.0	V	1, 2
Input voltage	V_t	-0.3 to $V_{CC} + 0.3$	V	1
Operating temperature	T_{opr}	-30 to +75	°C	
Storage temperature	T_{stg}	-55 to +125	°C	4

Notes: * If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

DC Characteristics ($V_{CC} = 2.4\text{ V to }5.5\text{ V}$, $T_a = -30\text{ to }+75^\circ\text{C}^*_{3}$)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage (1) (except OSC1)	VIH1	0.7VCC	—	VCC	V		5, 6
Input low voltage (1) (except OSC1)	VIL1	-0.3	—	0.2VCC	V	VCC=2.4 to 3.0V	5, 6
		-0.3	—	0.6	V	VCC=3.0 to 4.5V	
Input high voltage (2) (OSC1)	VIH2	0.7Vcc	—	Vcc	V		15
Input low voltage (2) (OSC1)	VIL2	—	—	0.2Vcc	V		15
Output high voltage (1) (D0–D7)	VOH1	0.75Vcc	—	—	V	-I _{OH} = 0.1 mA	7
Output low voltage (1) (D0–D7)	VOL1	—	—	0.2Vcc	V	I _{OL} = 0.1 mA	7
Output high voltage (2) (except D0–D7)	VOH2	—	—	—	V	-I _{OH} = 0.04 mA	8
Output low voltage (2) (except D0–D7)	VOL2	—	—	0.2Vcc	V	I _{OL} = 0.04 mA	8
Driver ON resistance (COM)	R _{COM}	—	—	20	k	I _d = 0.05 Ma VLCD = 4V	13
Driver ON resistance (SEG)	R _{SEG}	—	—	30	k	I _d = 0.05 mA, VLCD = 4V	13
I/O leakage current	I _{LI}	-1	—	1	A	VIN = 0 to V _{CC}	9
Pull-up MOS current (RESET* pin)	-I _p	5	50	120	A	V _{CC} = 3V VIN = 0V	
Power supply current	I _{CC1}	—	150	300	A	Rf oscillation, ernal clock VCC = 3V, fOSC = 215 kHz	10,14
	I _{CC2}	—	25	—	A	Sleep mode VCC = 3V fOSC = 215 kHz	
LCD voltage	VLCD	3.0	—	15.0	V	V _{CC} -V5	16

Booster Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Output voltage (V5OUT2 pin)	VUP2	8.2	8.9	—	V	$V_{CC} = V_{Ci} = 4.5V$, $I_o = 0.25\text{ mA}$, $C = 1\ \mu F$, $f_{osc} = 215\text{ kHz}$, $T_a = 25^\circ C$	18
Output voltage (V5OUT3 pin)	VUP3	7.2	7.8	—	V	$V_{CC} = V_{Ci} = 2.7V$, $I_o = 0.25\text{ mA}$, $C = 1\ \mu F$, $f_{osc} = 215\text{ kHz}$, $T_a = 25^\circ C$	18
Input voltage	V _{Ci}	1.0	—	5.0	V	$V_{Ci} \leq V_{CC}$	18, 19

AC Characteristics ($V_{CC} = 2.4V$ to $5.5V$, $T_a = -30$ to $+75^\circ C^*_{3}$)

Clock Characteristics ($V_{CC} = 2.7\text{ V}$ to 5.5 V , $T_a = -30$ to $+75^\circ C^*_{3}$)

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Notes
External Clock operation	External clock frequency	f_{cp}	80	215	350	kHz	$V_{CC} = 2.4$ to $2.7V$	11
			80	215	550	kHz	$V_{CC} = 2.7$ to $5.5V$	
	External clock duty	Duty	45	50	55	%		
	External clock rise time	t_{rcp}	—	—	0.2	μs		
	External clock fall time	t_{rcp}	—	—	0.2	μs		
R _f oscillation	Clock oscillation frequency(XD1602A0)	f_{osc}	110	150	200	kHz	$R_f = 150\text{ k}\Omega$, $V_{CC} = 3V$	12

System Interface Timing Characteristics (1) ($V_{CC} = 2.4V$ to $4.5V$, $T_a = -30$ to $+75^{\circ}C^{*3}$)

Bus Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{CYCE}	500	—	—	ns	Figure 50 $V_{CC} = 2.4$ to $3.0V$ $V_{CC} = 3.0$ to $4.5V$ Figure 50
Enable pulse width (high level)	PW_{EH}	250 150	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/W to E)	t_{AS}	80	—	—		
Address hold time	t_{AH}	20	—	—		
Data set-up time	t_{DSW}	140	—	—		
Data hold time	t_H	30	—	—		

Bus Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{CYCE}	1000	—	—	ns	Figure 51
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/W to E)	t_{AS}	60	—	—		
Address hold time	t_{AH}	20	—	—		
Data set-up time	t_{DSW}	—	—	360		
Data hold time	t_H	5	—	—		

Serial Interface Sequence

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	t_{SCYC}	1	—	20	μs ns	Figure 52
Serial clock (high level width)	t_{SCH}	400	—	—		
Serial clock (low level width)	t_{SCL}	400	—	—		
Serial clock rise/fall time	t_{scr}, t_{scf}	—	—	50		
Chip select set-up time	t_{CSU}	60	—	—		
Chip select hold time	t_{CH}	200	—	—		
Serial input data set-up time	t_{SISU}	200	—	—		
Serial input data hold time	t_{SIH}	200	—	—		
Serial output data delay time	t_{SOD}	—	—	360		
Serial output data hold time	t_{SOH}	5	—	—		

System Interface Timing Characteristics (2) ($V_{CC} = 4.5V$ to $5.5V$, $T_a = -30$ to $+75^{\circ}C^{*3}$)

Bus Write Operation

Item	Symbol	Min	Typ	Max	Unit
Enable cycle time	t _{CYCE}	500	—	—	ns Figure 50
Enable pulse width (high level)	PW _{EH}	150	—	—	
Enable rise/fall time	t _{Er} , t _{Ef}	—	—	20	
Address set-up time (RS, R/W to E)	t _{AS}	40	—	—	
Address hold time	t _{AH}	30	—	—	
Data set-up time	t _{DSW}	80	—	—	
Data hold time	t _H	30	—	—	

Bus Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t _{CYCE}	500	—	—	ns	Figure 51
Enable pulse width (high level)	PW _{EH}	230	—	—		
Enable rise/fall time	t _{Er} , t _{Ef}	—	—	20		
Address set-up time (RS, R/W to E)	t _{AS}	40	—	—		
Address hold time	t _{AH}	30	—	—		
Data set-up time	t _{DSW}	—	—	160		
Data hold time	t _H	5	—	—		

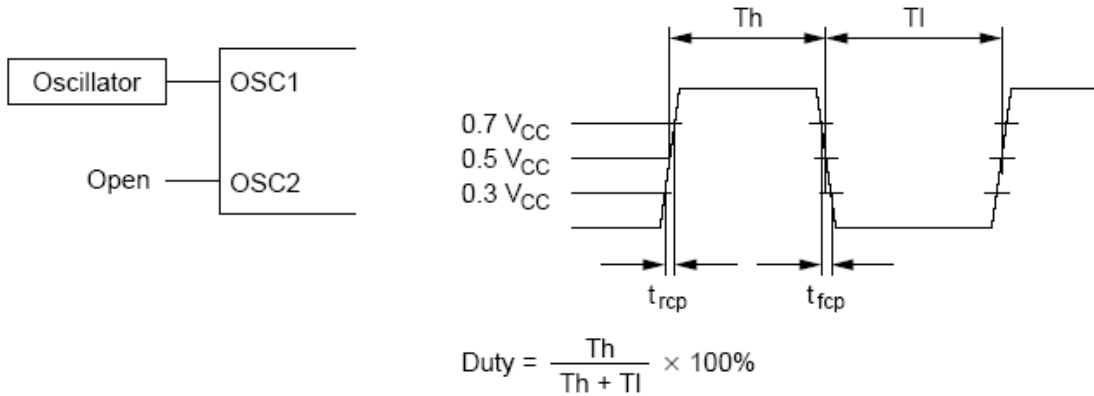
XD1602A0 Segment Extension Signal Timing Characteristics ($V_{CC} = 2.4V$ to $5.5V$, $T_a = -30$ to $+75^\circ C^*_{(3)}$)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	800	—	—	ns Figure 53
	Low level	t_{CWL}	800	—	—	
Clock set-up time	t_{CSU}	500	—	—		
Data set-up time	t_{SU}	300	—	—		
Data hold time	t_{DH}	300	—	—		
M delay time	t_{DM}	-1000	—	1000		
COMD set-up time	t_{DSU}	300	—	—		
Clock rise/fall time	COMD	t_{cl1}	—	—	700	
	Pins except COMD	t_{cl2}	—	—	200	

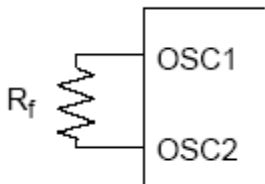
Reset Timing Characteristics ($V_{CC} = 2.4V$ to $5.5V$, $T_a = -30$ to $+75^\circ C^*_{(3)}$)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reset low-level width	t_{RES}	10	—	—	ms	Figure 54

- 10. Input/output current is excluded. When input is at an intermediate level with CMOS, the excessive current flows through the input circuit to the power supply. To avoid this from happening, the input level must be fixed high or low.
- 11. Applies only to external clock operation.

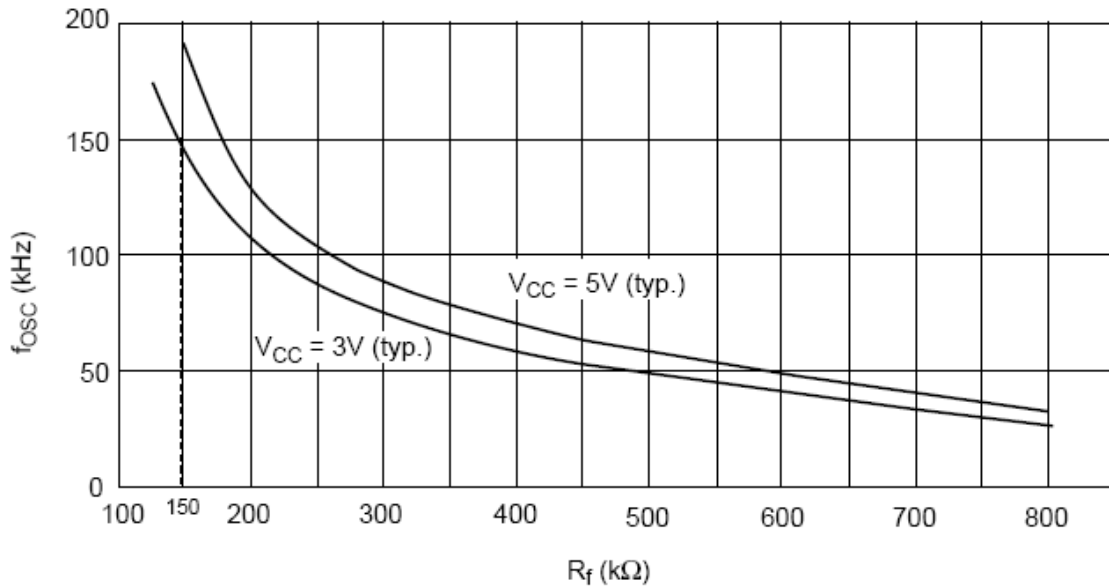


- 12. Applies only to the internal oscillator operation using oscillation resistor R_f .



Recommended resistor value
 R_f : 150k $\pm 2\%$ (When $V_{CC} = 3V$ to 4V)
 R_f : 180k $\pm 2\%$ (When $V_{CC} = 4V$ to 5V)

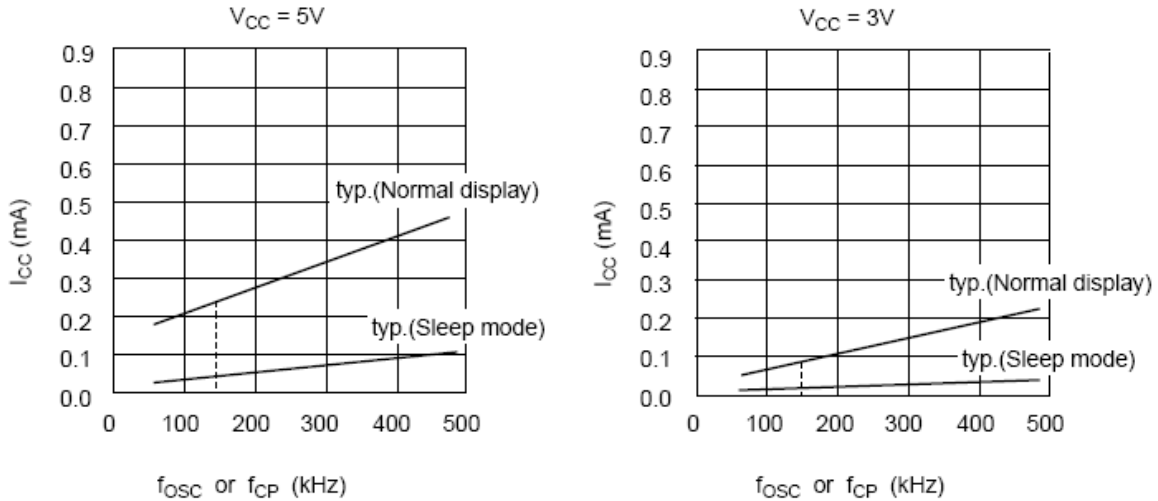
Since oscillation frequency varies depending on OSC1 and OSC2 terminal capacitance, wiring length to these pins should be minimized.



13. RCOM is the resistance between the power supply pins (V_{CC} , V1, V4, V5) and each common signal pin (COM0 to COM25).

RSEG is the resistance between the power supply pins (V_{CC} , V2, V3, V5) and each segment signal pin (SEG1 to SEG191).

14. The following graphs show the relationship between operation frequency and current consumption (referential data).

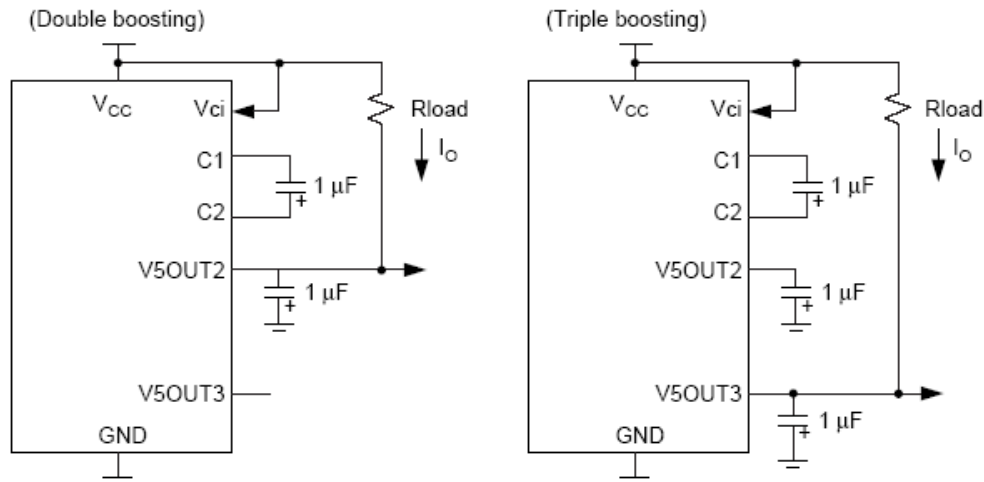


15. Applies to the OSC1 pin.

16. Each COM and SEG output voltage is within $\pm 0.15V$ of the LCD voltage (V_{CC} , V1, V2, V3, V4, V5) when there is no load.

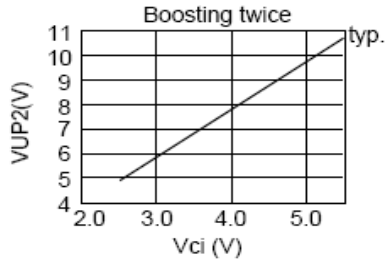
17. The TEST pin must be fixed to ground, and the IM pin must also be connected to V_{CC} or ground.

18. Booster characteristics test circuits are shown below.

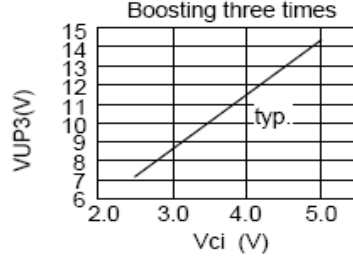


$VUP2 = V_{CC} - V5OUT2$ $VUP3 = V_{CC} - V5OUT3$

(i) VUP2, VUP3 vs Vci

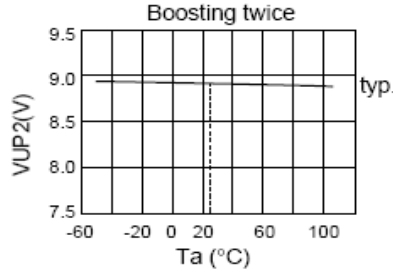


Test condition : Vci=V_{CC}, f_{cp}=140kHz, Ta=25°C

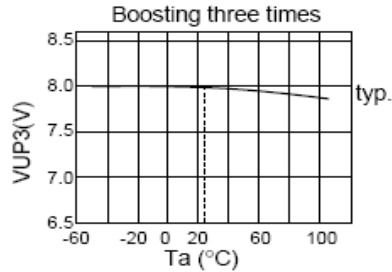


Test condition : Vci=V_{CC}, f_{cp}=140kHz, Ta=25°C

(ii) VUP2, VUP3 vs Ta

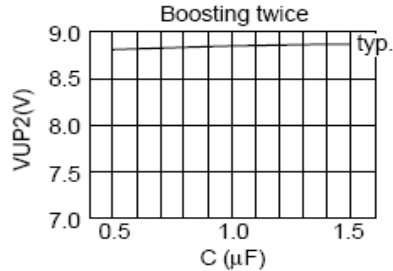


Test condition : Vci=V_{CC}=4.5V, R_f=180kΩ, I_o=0.1mA

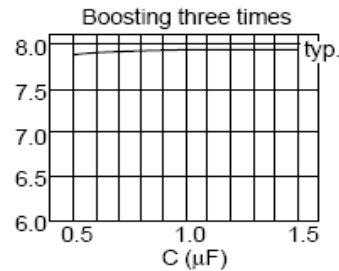


Test condition : Vci=V_{CC}=2.7V, R_f=150kΩ, I_o=0.1mA

(iii) VUP2, VUP3 vs Capacitance

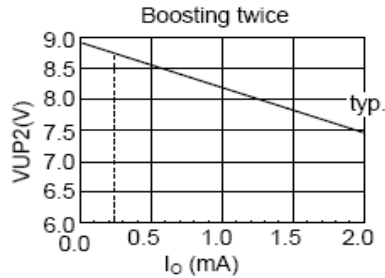


Test condition : Vci=V_{CC}=4.5V, R_f=180kΩ, I_o=0.1mA

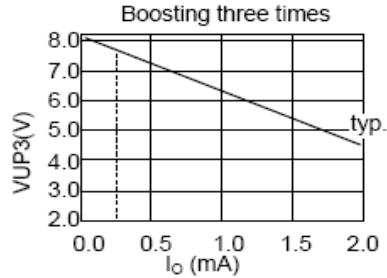


Test condition : Vci=V_{CC}=2.7V, R_f=150kΩ, I_o=0.1mA

(iv) VUP2, VUP3 vs I_o



Test condition : Vci=V_{CC}=4.5V, R_f=180kΩ, Ta=25°C

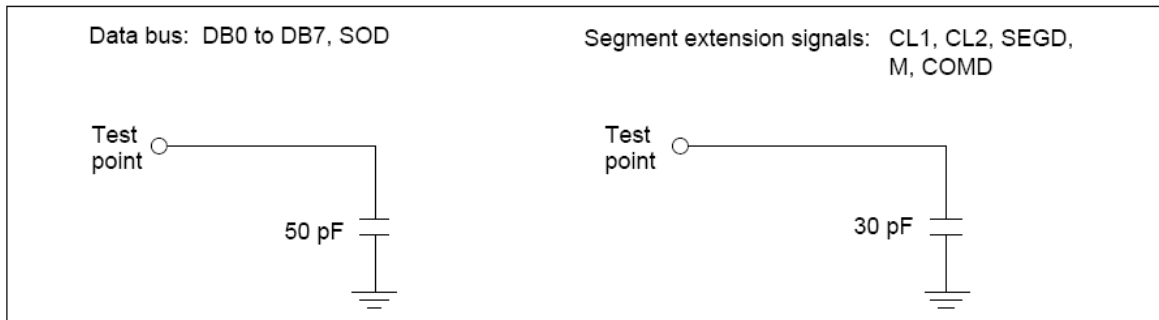


Test condition : Vci=V_{CC}=2.7V, R_f=150kΩ, Ta=25°C

19. Vci ≤ Vcc must be maintained.

Load Circuits

AC Characteristics Test Load Circuits



Timing Characteristics

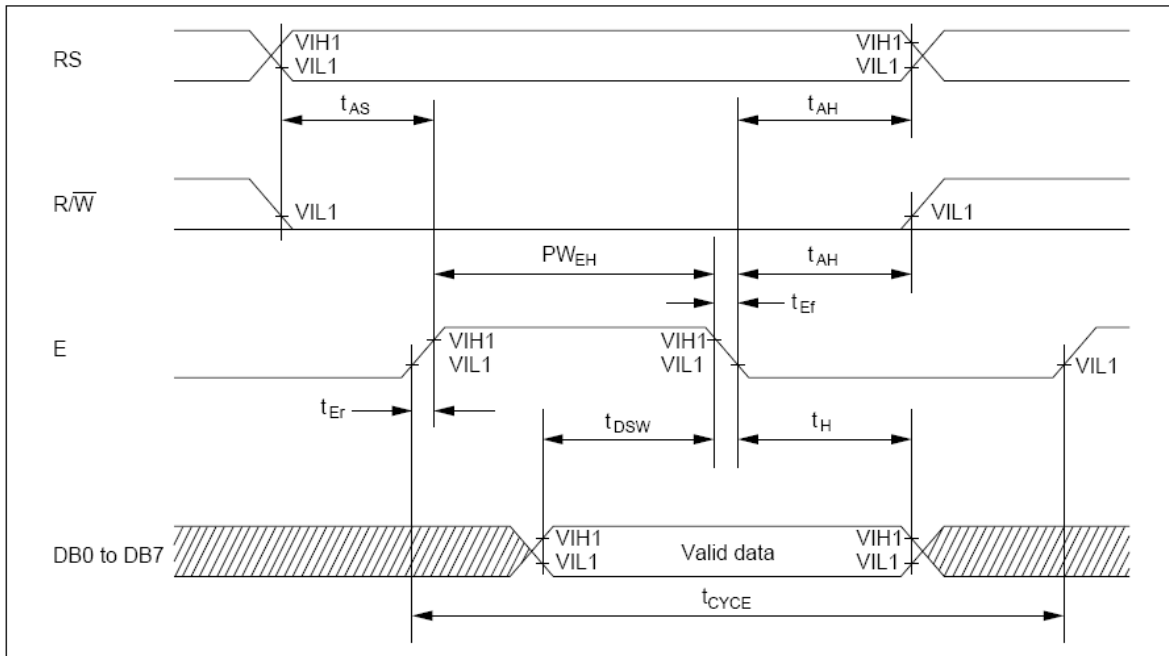


Figure 50 Bus Write Operation

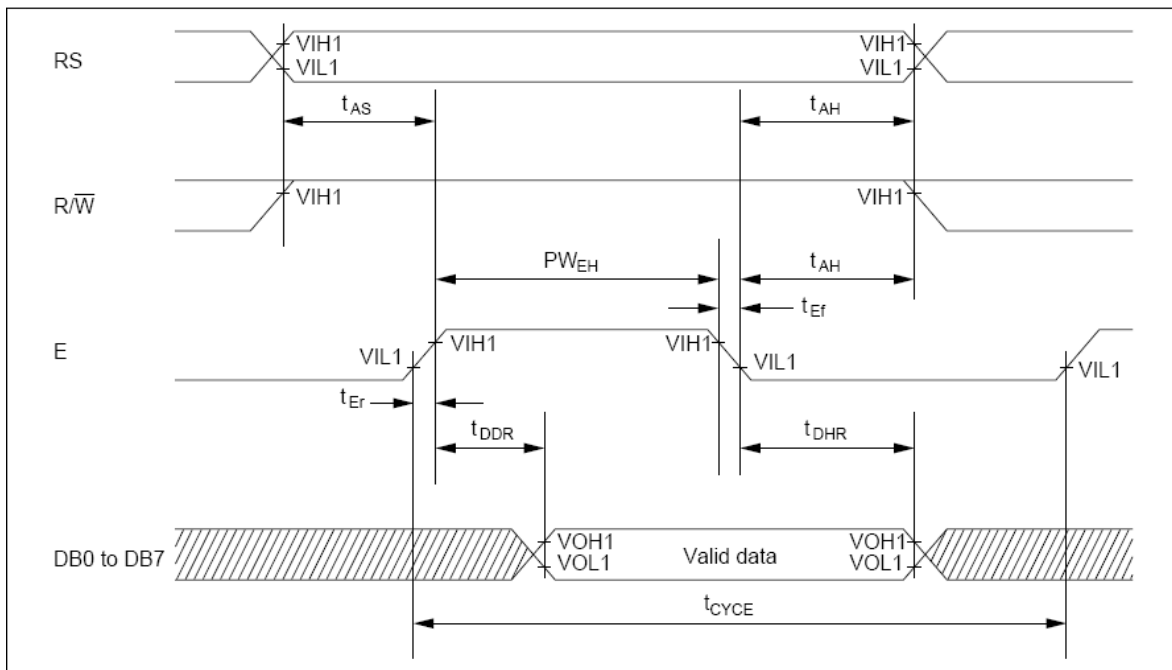


Figure 51 Bus Read Operation

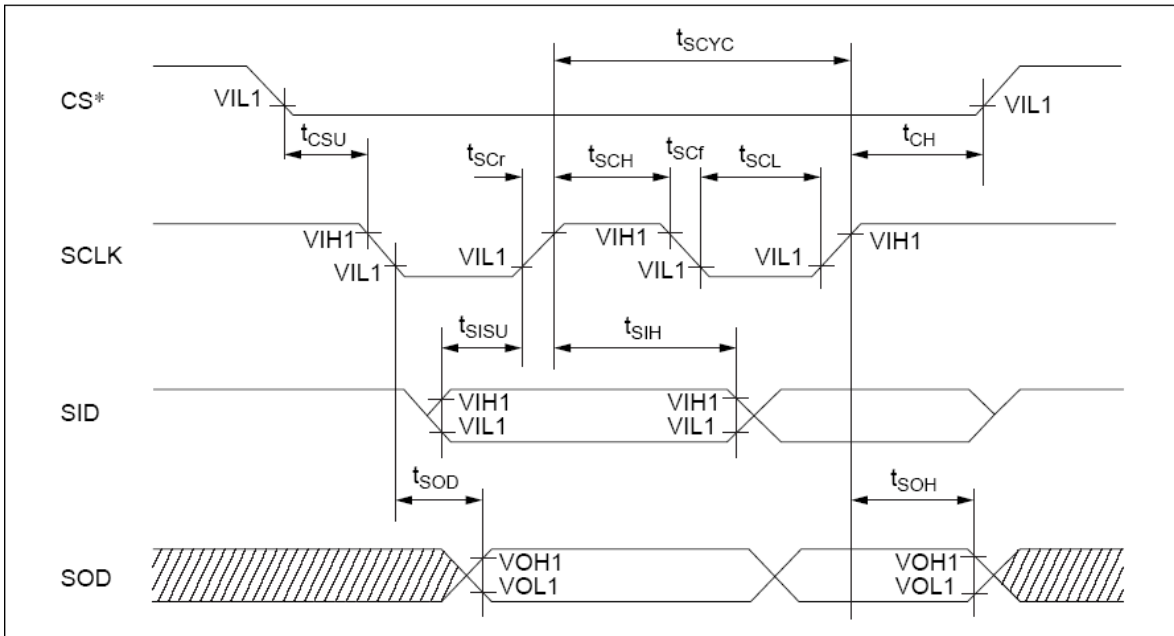


Figure 52 Serial Interface Timing

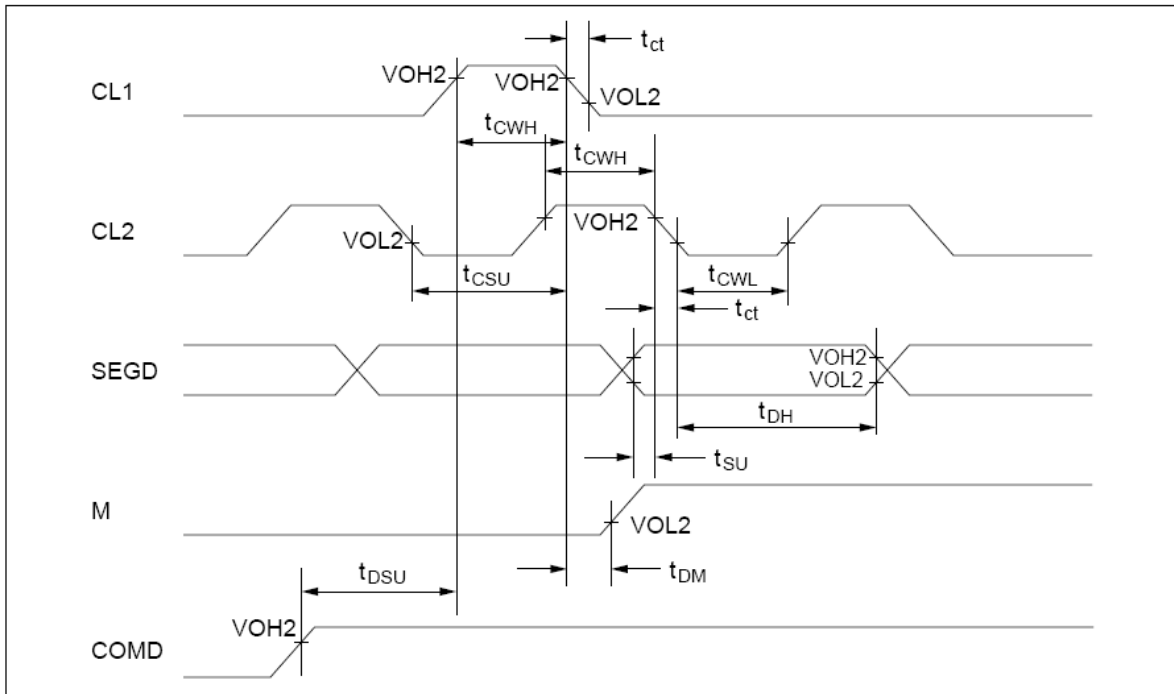


Figure 53 Interface Timing with Extension Driver

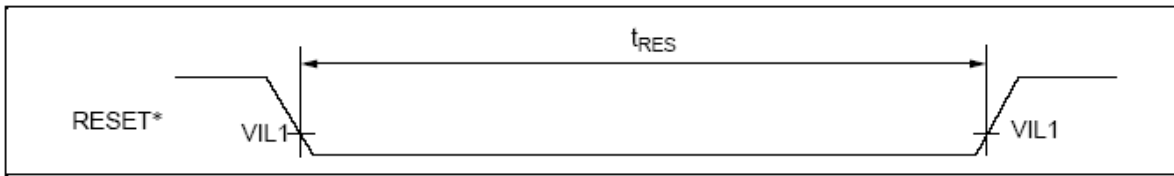


Figure 54 Reset Timing

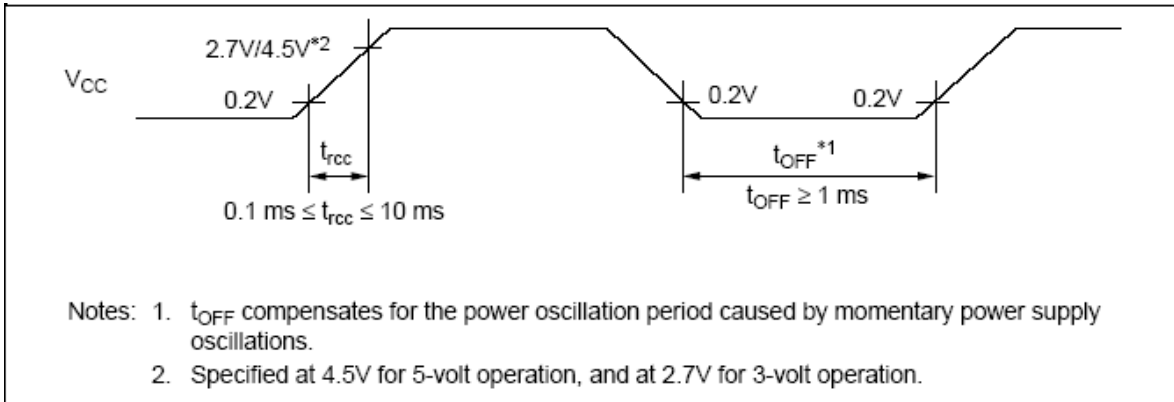


Figure 55 Power Supply Sequence